Audit Course-4

Instrumentation and Power Lab

Instrumentation

List of Experiments: (Any 8 experiments)

1. Weight measurement using load cell and strain gauges.
2. Measurement of vibration.
3. Liquid level measurement (Capacitance probe/ Ultrasonic/Hydrostatic-any one technique)
4. Flow measurement with orifice plate and differential pressure transmitter (DPT).
5. Measurement of speed of rotation of shaft using optical incremental encoder.
6. Temperature measurement. (RTD signal conditioning with bridge circuit, instrumentation amplifier, ADC and microcontroller)
7. Simulation of temperature measurement experiment with anysoftware's (RTD signal conditioning with bridge circuit, instrumentation amplifier, ADC and microcontroller)
8. Determine RTD characteristic and find the sensitivity PT 100/500
9. Determine thermistor or Thermocouple characteristic and find its sensitivity.
10. Design of signal converters using Electronics/electro-mechanical components (any one out of V/I, I/V, I/P, P/I)
11. Pneumatic cylinder sequencing with simple logic.
12. Data acquisition and analysis using PC.
13. Study of various switches
14. Study of different valves and their characteristics.
15. Study of characteristics of valves

Power Electronics

Lab setup requirement:

PMLK Buck Kit, PMLK LDO Kit, DC power supply 0-50V/4A with dynamic voltage mode capability ,5-100 ohm/50W resistance,2-100 ohm potentiometer/50 W , 4 digital multimeters with 4 1/2-digit resolution ,250MHz 2-channels Digital Oscilloscope,10 MHz Function Generator.

List of Experiments:

1. Single phase Semi / Full Converter with R & R-L load
2. Three phase Semi / Full Converter with R load
3. Single phase AC voltage controller using SCRs for R load
4. Single-Phase PWM bridge inverter for R load
5. Three-Phase inverter for R load
6. With TPS7A4901 and TPS7A8300, study-
   i. Impact of line and load conditions on drop out voltage
   ii. Impact of line and load conditions on efficiency
   iii. Impact of capacitor on PSRR

iv. Impact of output capacitor on load-transient response

7.Study of DC-DC Buck converter

v. Analyze the influence of voltage loop feedback compensation on load-transient response of current-mode control TPS54160 buck regulator.
vi. Analyze the way the operating conditions influence the current ripple and voltage ripple of a TPS54160 buck regulator, depending on the type of core material of the inductor and on core saturation..

8.Study of DC-DC Boost Converter

a. Analyze the influence of Input voltage, load current and switching frequency on continuous and discontinuous mode of operation of boost converter LM5122
b. Analyze the impact of operating conditions and of the operation mode on the power loss and efficiency of boost converter LM5122

9. Case study of any one of the following: HVDC transmission system, Photovoltaic System, Wind generator system

10. **Webench Experiment:**

Design Statement 1:

Design a low cost synchronous buck converter

Vin (Max): 15 V Vout: 5 V

Vin (Min): 10 V Iout: 1 A

Ambient Temp: 30°C

Ambient temperature: 30 degree Celsius

- IC should be a synchronous step down regulator
- IC should operate in advance eco-mode
- The efficiency should be greater than 90%
- Foot print should be less than 130mm2
- BOM cost should be less than 2$ and the solution should have lowest BOM cost
- BOM count should be less than 10
- Should consist of Maximum WEBENCH tools (minimum 5 tools)
- IC should support a soft start feature
- Design should not exceed 50 Degree Celsius Temperature at IC-Die (use thermal simulation
- optimization if required)

Design Statement 2:

Vin(Min) = 8 V Vin(Max) = 16 V

Vout = 5 V Iout = 2 A

Ambient temperature: 30 Degree Celsius

Design must support these four Webench tools (Electrical Simulation ,WebTherm, CAD Export, Schematic Editor)

IC must have frequency synchronization pin to reduce EMI

Frequency of the design must be less than 300KHz

Efficiency of the design should be above 85%

Foot print size should be less than 450mm2
The design maximum output voltage Vout Max(V) should be 42V DC
The minimum input voltage Vin Min(V) should be equal to 6.0V DC
Highest temperature on the PCB should be less than 40 Degree Celsius (use thermal simulation optimization as required)
Design should have better transient response for Load current
The design should have low BOM cost
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References:

- PMLK BUCK Lab manual - http://www.ti.com/lit/ug/ssqu007/ssqu007.pdf
- PMLK LDO Lab manual - http://www.ti.com/lit/ug/ssqu006/ssqu006.pdf
- WEBENCH – www.ti.com/webench
- ASLK PRO – ASLK PRO Manual