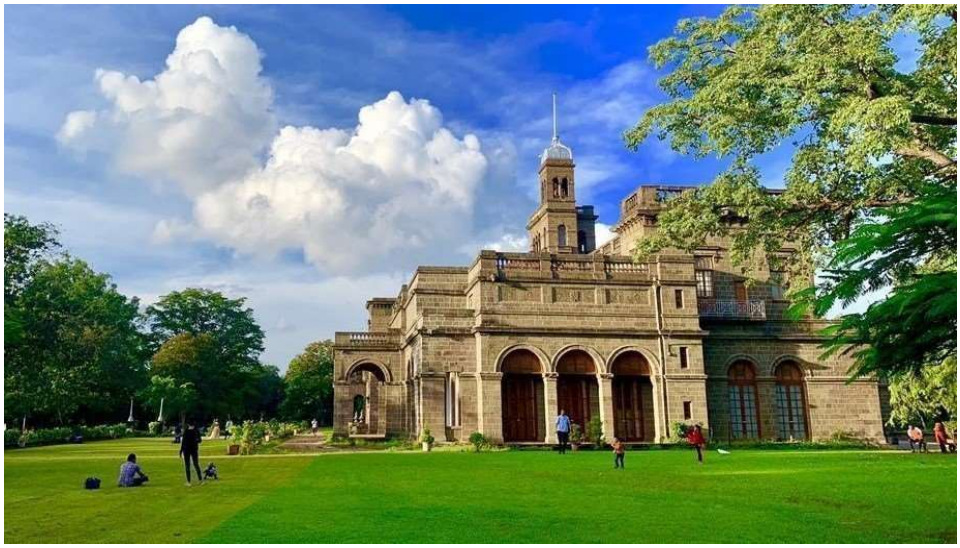
Savitribai Phule Pune University, Pune

Maharashtra, India

Faculty of Science and Technology,

BoS- Electronics & Telecommunication Engineering

National Education Policy (NEP)-2020 Compliant Curriculum



Honor Course in

VLSI and Chip Design Technology

Applicable from: Third Year (T.E.) for

1. **T.E. - E &TC Engineering**
2. **T.E. - Internet of Things (IoT)**
3. **T.E - Electronics & Computer Engineering**
4. **T.E. – Electronics Engineering (VLSI Design & Technology)**
5. **T.E. - Electronics & Comm. Engg. (Advanced Comm. Tech)**

(With effect from Academic Year 2026-27)

Preface by Board of Studies - Electronics & Telecommunication Engineering

Dear Students and Teachers,

It gives me immense pleasure to present the Honor Course in VLSI and Chip Design Technology for the under-graduate students of E&TC / VLSI Design & Technology / IoT / Advanced Communication Technology / Electronics & Computer Engineering under the Faculty of Science and Technology of Savitribai Phule Pune University. This course has been designed in alignment with the vision of the National Education Policy (NEP) 2020, emphasizing multidisciplinary learning, innovation, skill development, and industry-oriented education.

In the contemporary digital era, the rapid evolution of technology has made VLSI and chip design the backbone of virtually every electronic system, driving innovation across communication, computing, automotive, healthcare, and artificial intelligence. While this technological transformation has unlocked unprecedented opportunities for innovation, it has simultaneously created a growing demand for skilled professionals capable of designing, optimizing, and fabricating next-generation semiconductor devices and integrated circuits.

Under the aegis of the Board of Studies (BoS) in Electronics & Telecommunication Engineering, this curriculum for the Honors Course in VLSI and Chip Design Technology has been meticulously designed for Third Year (TE) and Final Year (BE) engineering students. The primary objective of this specialized program is to bridge the gap between traditional electronics and computer engineering education and the highly specialized, rapidly evolving domain of semiconductor and chip design technology.

I sincerely appreciate the valuable contributions of subject experts, academicians, industry professionals, and members of the Board of Studies who have devoted their expertise and efforts in framing this progressive curriculum. I am confident that this Honor Course will serve as a strong platform for nurturing future-ready engineers capable of contributing meaningfully to the rapidly evolving VLSI and semiconductor ecosystem.

I extend my best wishes to all students and faculty members for the successful implementation of this Programme.

Dr. S. D. Shirbahadurkar
Chairman,
Board of Studies, Electronics & Telecommunication Engineering
Savitribai Phule Pune University

Members of Board of Studies– E&TC Engineering	
Dr. Aditya Abhyankar	Dr. Rawal Awale
Dr. Bhagwat Jadhav	Dr. M.B. Mali
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Honor Course in VLSI and Chip Design Technology

Preamble

The semiconductor industry is one of the key drivers of technological advancement and economic growth worldwide. Semiconductors form the foundation of modern electronic systems and are indispensable in applications such as Artificial Intelligence (AI), Internet of Things (IoT), 5G/6G communication, high-performance computing, automotive electronics, consumer electronics, healthcare, Defence, aerospace, and industrial automation. With the Government of India's initiatives such as the India Semiconductor Mission (ISM) and the increasing establishment of semiconductor design centers and fabrication ecosystems, the need for engineers possessing specialized knowledge and skills in VLSI and Chip Design has grown significantly.

To address this emerging requirement, Savitribai Phule Pune University (SPPU) offers the Honors Programme in VLSI and Chip Design Technology as a multidisciplinary value-added Programme for undergraduate engineering students. The Programme is designed to complement the regular B.E./B.Tech curriculum by providing advanced knowledge and practical exposure in semiconductor technology, integrated circuit design, and VLSI system development. It aims to bridge the gap between academic learning and industry expectations by developing competencies required in the semiconductor ecosystem.

In alignment with the University Grants Commission (UGC) Curriculum and Credit Framework for Undergraduate Programme (CCFUP), National Education Policy (NEP) 2020, National Credit Framework (NCRF), and All India Council for Technical Education (AICTE) model curriculum guidelines, Savitribai Phule Pune University (SPPU) introduces Honors Courses in Engineering to promote multidisciplinary learning, advanced specialization, innovation, employability, entrepreneurship, and research orientation among undergraduate engineering students.

The Honors framework aims to:

- Provide domain specialization beyond the core engineering curriculum.
- Enhance industry readiness and interdisciplinary competence.
- Encourage research, innovation, and experiential learning.
- Support flexible and learner-centric education envisioned in NEP 2020.
- Facilitate pathways towards higher education, entrepreneurship, and emerging technologies.

About the Honors Programme

The Honors Programme in VLSI and Chip Design Technology is a structured, industry-aligned curriculum offered to students enrolled in E & TC Engg, Internet of Things (IoT), Electronics & Computer Engg, Electronics Engg. (VLSI Design & Technology), Electronics & Comm. Engg. (Advanced Comm. Tech.) and allied engineering disciplines. Commencement from the Semesters V through VIII, the Programme delivers one theory course and one laboratory-based practical course per semester, culminating in a capstone project, total four theory courses & four practical's with project, 18 credits overall.

The curriculum has been carefully designed in response to evolving National and International workforce demand projections for 2026–2030, preparing graduates to take on high-impact roles across RTL design & verification, physical design, analog & mixed-signal design, semiconductor fabrication, embedded systems, and design automation.

Employability Alignment (2026–2030 Boom Areas)

According to NASSCOM, India Semiconductor Mission (ISM) reports, and global semiconductor workforce studies, the following domains will see explosive demand through 2030:

- RTL Design & Verification — Sustained double-digit Year-over-Year growth in hiring across design houses
- Physical Design & Static Timing Analysis (STA) — High demand with a global shortage of skilled engineers
- Analog & Mixed-Signal (AMS) Design — Niche, high-value skillset; <5% of engineers qualified globally
- DFT (Design for Testability) Engineers — Critical for silicon yield and reliability at advanced nodes
- Embedded Systems & SoC Integration — Mandatory across automotive, telecom, and consumer electronics sectors
- EDA Tool Proficiency (Synopsys, Cadence, Mentor) — Essential across the entire semiconductor design flow
- Semiconductor Fabrication & Process Engineering — Expanding rapidly with new fabs under the ISM initiative.

Upon successful completion of the Honours Programme in VLSI and Chip Design Technology, graduates enter the global workforce equipped not only with technical expertise but also with the design and problem-solving capabilities required to address evolving semiconductor industry challenges. Their careers begin with foundational roles such as Junior Design Engineer, RTL/Verification Engineer, and Layout Design Engineer — critical positions that form the backbone of modern semiconductor design operations. As they gain experience, graduates can pursue specialized pathways across the front-end and back-end domains of chip design.

The front-end design track prepares professionals for high-demand roles including RTL Design Engineer, Functional Verification Engineer, Design Verification (DV) Specialist, and SoC Integration Engineer. The back-end design track develops expertise for Physical Design Engineer, STA Engineer, DFT Engineer, and Analog/Mixed-Signal Layout Designer roles.

For those drawn to fabrication and process technology, advanced opportunities exist in Process Integration, Semiconductor Device Engineering, and Fab Process Engineering — fields experiencing significant growth due to the expansion of India's fabrication ecosystem under the ISM. Recognizing the future direction of the industry, the Programme places special emphasis on the decade's fastest-growing disciplines: Advanced Node Design and AI-driven Chip Design. Graduates are prepared for roles such as SoC Design Architect, EDA Tools Specialist, Embedded Systems Engineer, and Semiconductor Process Engineer, with clearly defined pathways toward senior leadership positions including Principal Design Engineer and ultimately Chief Technology Officer (CTO) in semiconductor organizations.

A major emphasis of the Programme is on experiential and outcome-based learning. Students are provided with opportunities to develop practical skills through laboratory experiments, simulation-based learning, design assignments, mini-projects, and the use of industry-standard Electronic Design Automation (EDA) tools. The Programme also encourages interaction with semiconductor industries through expert lectures, workshops, internships, and collaborative projects, thereby enhancing employability and professional competence.

Pune has emerged as a major hub for semiconductor design and Global Capability Centers (GCCs), offering students significant opportunities for industrial exposure and career growth. The Honors Programme leverages this ecosystem to familiarize students with current industry practices and emerging semiconductor technologies.

Aligned with workforce projections for 2026–2030 — an era marked by rapid expansion of India's semiconductor design and fabrication ecosystem, heightened digital transformation, and the growth of Global Capability Centers — this Programme ensures graduates do not simply enter the semiconductor profession. They enter it prepared to design, innovate, and contribute meaningfully to India's vision of achieving global leadership and self-reliance in semiconductor technology.

General Rules and Guidelines

- An Honors Degree in Engineering shall mean an undergraduate engineering degree with -additional specialization credits earned by a student in the same or allied discipline beyond the regular B.E./B.Tech curriculum requirements.
- Honor program will commence in Semester V and will be spread over 4 semesters (V-VIII). Eligible students can opt for any one Honors or Minors certification offered in given academic year by the department. To avail Honors or Minors certification, students need to acquire additional 1 8 - 20 credits
- Eligibility: A student shall be eligible to register for an Honors Programme subject to the following conditions:

Sr.	Criteria	Requirement
1	Academic Eligibility	Passed all courses up to previous Semesters
2	Minimum CGPA	7.50 CGPA or above at the end of Second Year
3	Backlog Condition	No active backlog at the time of registration
4	Attendance	Minimum 75% attendance in regular Programme
5	Conduct	Good academic and disciplinary record

- The institute may relax the CGPA criterion in exceptional cases with approval of the Director/Principal
- It is absolutely not mandatory to any student to opt for Honors or Minors Program.
- Choice is given to individual student to undertake Honors/Minors programs from the third year engineering (Fifth Semester) to fourth year engineering (Eighth Semester)
- The registration for Honors /Minors Programme will lead to gain additional credits to such students.
- As per the standard practice, SGPA and CGPA calculations will be done with common base only by considering mandatory credits assigned for the Bachelor Programme as per the structure approved by the Academic Council SPPU.

Guidelines for Examination Scheme

Theory Examination: The theory examination shall be conducted in two different parts

Comprehensive Continuous Evaluation (CCE) and End-Semester Examination (ESE).

Comprehensive Continuous Evaluation (CCE) :

1. CCE of 30 marks based on all the Units of course syllabus to be scheduled and conducted at institute level.
2. Case studies included under each unit are intended to support applied learning and are part of Comprehensive Continuous Evaluation
3. These case studies will be assessed through internal assessment components such as presentations, assignments, or group discussions. They shall not be included in the End-Semester Theory Examination.
4. To design a Comprehensive Continuous Evaluation scheme for a theory subject of 30 marks with the specified parameters, the allocation of marks and the structure can be detailed as follows:

Sr.	Parameters	Marks	Coverage of Units
1	Unit Test	12 Marks	Units 1 & Unit 2 (6 Marks/Unit)
2	Assignments / Case Study	12 Marks	Units 3 & Unit 4 (6 Marks/Unit)
3	Seminar Presentation / Open Book Test/ Quiz	06 Marks	Unit 5

Format and Implementation of Comprehensive Continuous Evaluation (CCE)

- **Unit Test**
  - **Format :** Questions designed as per Bloom's Taxonomy guidelines to assess various cognitive levels (Remember, Understand, Apply, Analyze, Evaluate, Create).
  - **Implementation**: Schedule the test after completing Units 1 and 2. Ensure the question paper is balanced and covers key concepts and applications.
- **Assignments / Case Study** : Students should submit one assignment or one Case Study Report based on Unit 3 and one assignment or one Case Study Report based on Unit 4.
  - **Format:** Problem-solving tasks, theoretical questions, practical exercises, or case studies that require in-depth analysis and application of concepts.
  - **Implementation:** Distribute the assignments or case study after covering Units 3 and 4. Provide clear guidelines and a rubric for evaluation.
- **Seminar Presentation:**
  - **Format:** Oral presentation on a topic from Unit 5, followed by a Q&A session.
  - **Deliverables:** Presentation slides, a summary report in 2 to 3 pages, and performance during the presentation.
  - **Implementation:** Schedule the seminar presentations towards the end of the course. Pro-vide students with ample time to prepare and offer guidance on presentation skills.
- **Open Book Test:**
  - **Format:** Analytical and application-based questions to assess depth of understanding.

- **Implementation:** Schedule the open book test towards the end of the course, ensuring it covers critical aspects of Unit 5.

- **Quiz :**

  - **Format:** Quizzes can help your students practice existing knowledge while stimulating in-terest in learning about new topic in that course. You can set your quizzes to be completed individually or in small groups.
  - **Implementation:** Online tools and software can be used create quiz. Each quiz is made up of a variety of question types including multiple choice, missing words, true or false etc

- **Evaluation and Feedback:**

  - **Unit Test:** Evaluate promptly and provide constructive feedback on strengths and areas for improvement.
  - **Assignments / Case Study:** Assess the quality of submissions based on the provided rubric. Offer feedback to help students understand their performance.
  - **Seminar Presentation:** Evaluate based on content, delivery, and engagement during the Q&A session. Provide feedback on presentation skills and comprehension of the topic.
  - **Open Book Test**: Evaluate based on the depth of analysis and application of concepts. Provide feedback on critical thinking and problem-solving skills.

End-Semester Examination (ESE)

End-Semester Examination (ESE) of 70 marks written theory examination based on all the unit of course syllabus scheduled by university. Question papers will be sent by the University through QPD (Question Paper Delivery). University will schedule and conduct ESE at the end of the semester.

- **Format and Implementation:**

  - **Question Paper Design:** Below structure is to be followed to design an End-Semester Examination (ESE) for a theory subject of 70 marks on all 5 units of the syllabus with questions set as per Bloom's Taxonomy guidelines and 14 marks allocated per unit.

  - **Balanced Coverage**: Ensure balanced coverage of all units with questions that assess differ-ent cognitive levels of Bloom's Taxonomy: Remember, Understand, Apply, Analyze, Evaluate, and Create. The questions should be structured to cover:

  - **Detailed Scheme for 70 Marks:** Unit-Wise Allocation (14 Marks per Unit- as per the regular structure of mandatory course): Each unit will have a combination of questions designed to assess different cognitive levels. By following this scheme, you can ensure a comprehensive and fair assessment of students' understanding and application of the course material, adhering to Bloom's Taxonomy guidelines for cognitive skills evaluation.

NEP 2020 Compliant Curriculum Structure

Third & Final year Engineering (2024 Pattern)

Board: Electronics & Telecommunication Engineering

Curriculum Structure for Honor in VLSI and Chip Design Technology

Year & Semester	Course Code	Course Name	Teaching Scheme		Examination Scheme					Credits		
			Theory	Practical	CCE	ESE	Term Work	Oral	Total	Theory	Practical	Total
T.E. – V	HVT 301ETC	Digital VLSI CHIP Design	3	-	30	70	-	-	100	3	-	3
	HVT 302 ETC	Logic Synthesis and Verification Lab		2			25	25	50		1	1
T.E. – VI	HVT 351 ETC	Analog VLSI CHIP Design	3	-	30	70	-	-	100	3	-	3
	HVT 352 ETC	Schematic Capture and SPICE Simulation Lab		2	-	-	25	25	50	-	1	1
B.E. – VII	HVT 401 ETC	Automated Physical Design	3		30	70	-		100	3		3
	HVT 402 ETC	ASIC Implementation Flow Lab		2	-	-	25	25	50	-	1	1
B.E. – VIII	HVT 451 ETC	Custom Layout	3	-	30	70	-	-	100	3	-	3
	HVT 452 ETC	Physical Verification and Extraction Lab		2	-	-	25	25	50	-	1	1
	HVT 453 ETC	Honors Project	-	4			50	50	100		2	2
Total			**12**	**12**	**120**	**280**	**100**	**100**	**700**	**12**	**6**	**18**

Savitribai Phule Pune University **Honor in VLSI and Chip Design Technology**		
HVT 301 ETC - Digital VLSI CHIP Design		
Teaching Scheme	**Credits**	**Examination Scheme**
Theory : 03 Hours/Week	03	CCE : 30 Marks End-Semester: 70 Marks

Course Objectives: The course aims to:

1. Explain fundamental understanding of VLSI and digital IC design.
2. Develop detail understanding of hardware description languages.
3. Analyze Digital VLSI chip designs proficiency in Verilog/VHDL syntax and semantics.
4. Enable students to apply procedures, tasks, functions, and memory modeling techniques in Verilog/VHDL.
5. Evaluate and implement practical digital designs using HDL-based techniques.

Course Outcomes: Upon successful completion of this course, students will be able to:

- CO1: Analyze fundamental concepts of VLSI and digital IC design, and VLSI design methodologies.
- CO2: Describe the principles of hardware description languages (Verilog/VHDL).
- CO3: Apply the syntax and semantics of Verilog/VHDL to design HDL-based digital circuits using procedures, tasks, functions, and memory modeling techniques.
- CO4: Implement and analyze digital circuits using concurrent and sequential constructs and Verilog/VHDL-based design methodologies.
- CO5: Design and model sequential circuits and finite state machines (FSMs) using Verilog/VHDL, and evaluate their functional behavior through simulation.

Course Contents

Unit I - Introduction to Digital VLSI Chip Design (09 Hours)

Introduction to VLSI and digital IC design, VLSI design flow, Full-custom, semi-custom, standard-cell design, ASIC design flow, ASIC and FPGA overview, FPGA architecture, Logic synthesis

Unit II - Fundamentals of HDL (09 Hours)

Basic concepts of hardware description languages, Gajski-Y chart, Design flow for VHDL/Verilog based RTL/logic synthesis. Hierarchy, Concurrency, Logic, and Delay modeling, Structural, Data-flow and Behavioral styles of hardware description. Architecture of event driven simulators.

Unit III – Insights of HDL (09 Hours)

Syntax and Semantics of Verilog/VHDL. Variable, signal types, arrays, attributes and tables. Data types, Operators, expressions and signal assignments. Entities, architecture specification, and configurations. Component instantiation.

Unit IV – Advancements of HDL (09 Hours)

Use of Procedures, Tasks and functions, Memory Modelling, Examples of design using Verilog/ VHDL.

Unit V – State Machines (09 Hours)

Concurrent and sequential constructs. Examples of design using Verilog. Sequential Circuit design, Finite State Machine Modeling.

Learning Resources

Text Books:

1. Verilog HDL: A Guide to Digital Design and Synthesis, S. Palnitkar, "Prentice Hall NJ, USA),1996
2. Advanced Digital Design with the Verilog HDL, Michael D. Ciletti, Prentice Hall India, 2005
3. VHDL: Analysis and Modeling of Digital Systems, Z. Navabi, McGraw Hill International Ed. 1998.
4. VHDL Primer, J. Bhaskar, Pearson Education Asia,2001.

Reference Books

1. Verilog Digital System Design, Z. Navabi, McGraw Hill Education 2nd Ed. 2008.
2. Fundamentals of Digital Logic with Verilog Design, Stephen Brown and Zvonko Vranesic, McGraw-Hill Higher Education.
3. Fundamentals of Digital Logic with VHDL Design, Stephen Brown and Zvonko Vranesic, McGraw-Hill Higher Education.

Recommended Certifications

1. https://onlinecourses.nptel.ac.in/e-learning/preview/noc21_ee09
2. https://nptel.ac.in/courses/117106092 https://nptel.ac.in/courses/117106092

Savitribai Phule Pune University **Honor in VLSI and Chip Design Technology**		
HVT 302 ETC - Logic Synthesis and Verification Lab		
Teaching Scheme	**Credits**	**Examination Scheme**
Practical : 02 Hours/Week	01	Term Work: 25 Marks Oral: 25 Marks

Course Objectives: The course aims to:

1. To provide hands-on exposure to VHDL/Verilog-based RTL design flow, from HDL coding to logic synthesis.
2. To develop practical skills in writing structural, data-flow, and behavioral style HDL descriptions of digital circuits.
3. To train students in using data types, operators, entities, architectures, and component instantiation through simulation-based design exercises.
4. To enable students to model digital designs using procedures, tasks, functions, and memory elements in Verilog/VHDL.
5. To provide practical experience in designing and verifying sequential circuits and finite state machines (FSMs) using simulation and synthesis tools.

Course Outcomes: Upon successful completion of this course, students will be able to:

- CO1: Write and simulate structural, data-flow, and behavioral style HDL models for combinational circuits.
- CO2: Apply Verilog/VHDL syntax — data types, operators, entities, architectures, and component instantiation — to design digital circuits.
- CO3: Model digital circuits using procedures, tasks, functions, and memory elements in Verilog/VHDL.
- CO4: Design and simulate circuits using concurrent and sequential constructs.
- CO5: Design, model, and verify sequential circuits and FSMs through simulation and logic synthesis.

List of Laboratory Experiments / Assignments

1. Study of HDL simulation/synthesis tool environment; write and simulate a basic combinational circuit (e.g., multiplexer/decoder) using structural style
2. Design and simulate combinational circuits using dataflow style (e.g., adder/comparator)
3. Design and simulate combinational circuits using behavioral style (e.g., ALU/priority encoder)
4. Design a digital circuit using procedures, tasks, and functions in Verilog/VHDL
5. Memory modeling: design and simulate a RAM/ROM module using behavioral constructs
6. Design and simulate sequential circuits (flip-flops, counters, shift registers) using concurrent and sequential constructs
7. Design and model a Finite State Machine (FSM) (e.g., traffic light controller/sequence detector) and verify functional behavior through simulation
8. Logic synthesis of an HDL design (any of the above) using a synthesis tool; analyze the synthesized gate-level netlist, area, and timing report

Savitribai Phule Pune University **Honor in VLSI and Chip Design Technology**		
HVT 351 ETC- Analog VLSI CHIP Design		
Teaching Scheme	**Credits**	**Examination Scheme**
Theory : 03 Hours/Week	03	CCE : 30 Marks End-Semester: 70 Marks

Course Objectives: The course aims to:

1. Study Basics of analog IC designing.
2. Analyze different analog amplifiers.
3. Understand the fundamental aspects of operational amplifiers.
4. Understand the Frequency response, stability and noise issues in amplifiers.
5. Evaluate the implementation of different comparators.

Course Outcomes: Upon successful completion of this course, students will be able to:

- CO1: Analyze the operating principles and characteristics of basic analog building blocks.
- CO2: Design basic amplifiers, differential amplifiers, cascade amplifiers, and high-gain amplifier structures for analog integrated circuit applications.
- CO3: Evaluate the characteristics and performance of operational amplifiers, and design basic op-amp circuits considering frequency response and compensation techniques.
- CO4: Analyze noise sources and biasing schemes in operational amplifiers, and design high-performance op-amps considering gain, bandwidth, stability, and noise.
- CO5: Analyze and design single-stage and two-stage comparators, comparators with hysteresis, and auto-zero circuits for reliable analog and mixed-signal applications.

Course Contents

Unit I – Introduction to Analog VLSI Chip Design (09 Hours)

Basic Analog Building Blocks, Switches, Active Resistors, Current and Voltage sources, Current Mirrors, Current and voltage references, Voltage regulators.

Unit II – Analog Amplifiers (09 Hours)

Amplifiers: Basic Amplifiers, Differential Amplifier, Cascade Amplifiers, High Gain Amplifier Structure, Amplifier design.

Unit III – Operational Amplifiers (09 Hours)

Operational Amplifiers: Operational Amplifier characteristics, Basic Op-Amp circuits, Frequency response and compensation.

Unit IV – Op-Amp Design and advancements (09 Hours)

Noise sources in Op-Amps, Op-Amp design including Biasing circuits, High performance Op-Amps.

Unit V – Comparators (09 Hours)

Comparators: Single stage comparators, Two stage comparator, Comparators with Hysteresis, Auto zero techniques.

Learning Resources

Text Books:

1. CMOS Analog Circuit Design" Phillip E. Allen and Douglas R. Holberg.
2. Principles of CMOS VLSI design: A system Perspective, Neil H.E. Weste and Kamran Eshraghian.

Reference Books

1. VLSI Design Techniques for Analog and Digital Circuits", Randall Geiger, Phillip E. Allen and Noel Stradder, McGraw Hill International Edition, McGraw Hill.

Recommended Certifications

1. https://nptel.ac.in/courses/108106105
2. https://onlinecourses.nptel.ac.in/e-learning/preview/noc23_ee142

Savitribai Phule Pune University **Honor Course in VLSI and Chip Design Technology**		
HVT 352 ETC- Schematic Capture and SPICE Simulation Lab		
Teaching Scheme	**Credits**	**Examination Scheme**
Practical : 02 Hours/Week	01	Term Work: 25 Marks Oral: 25 Marks

Course Objectives:

1. To provide hands-on exposure to schematic capture and SPICE simulation tools (e.g., Cadence Virtuoso/LTspice/PSpice) for analog circuit design.
2. To develop practical skills in designing and simulating basic analog building blocks such as current mirrors, active resistors, and voltage/current references.
3. To train students in designing and characterizing single-stage and multi-stage amplifiers, including differential and cascade configurations.
4. To enable students to design, simulate, and evaluate operational amplifiers considering frequency response, compensation, noise, and biasing.
5. To provide practical experience in designing and analyzing comparator circuits for analog and mixed-signal applications.

Course Outcomes (COs):

- CO1: Design and simulate basic analog building blocks (switches, active resistors, current mirrors, voltage/current references) using SPICE.
- CO2: Design and characterize basic, differential, and cascade amplifiers through schematic capture and simulation.
- CO3: Design an operational amplifier and evaluate its frequency response, gain, and compensation through SPICE simulation.
- CO4: Analyze noise sources and design appropriate biasing circuits for high-performance op-amp operation.
- CO5: Design and evaluate single-stage/two-stage comparators and comparators with hysteresis/auto-zero techniques for mixed-signal applications.

List of Assignment /Experiments

1. Study of schematic capture and SPICE simulation tool environment; simulate basic switches and active resistors
2. Design and simulate a current mirror circuit; analyze current-copying accuracy and output resistance
3. Design and simulate a voltage/current reference and a basic voltage regulator circuit
4. Design and simulate a basic (single-stage) amplifier; analyze gain, bandwidth, and biasing
5. Design and simulate a differential amplifier and a cascade amplifier; compare gain and output impedance.
6. Design a two-stage operational amplifier; simulate frequency response and analyze compensation techniques.

7. Analyze noise sources in the designed op-amp; simulate biasing circuits and evaluate high-performance op-amp parameters (gain, bandwidth, stability, noise).

8. Design and simulate a single-stage/two-stage comparator with hysteresis and auto-zero technique; analyze switching behavior and offset performance.

Savitribai Phule Pune University **Honor in VLSI and Chip Design Technology**		
HVT 401 ETC- Automated Physical Design		
Teaching Scheme	**Credits**	**Examination Scheme**
Theory : 03 Hours/Week	03	CCE: 30 Marks End-Semester: 70 Marks

Course Objectives: The course aims to:

1. To introduce the physical design flow from netlist to GDSII, covering floor planning and power planning.
2. To develop skills in placement and clock tree synthesis using automated EDA tools.
3. To impart techniques for global and detailed routing and congestion resolution.
4. To build competency in post-route timing analysis and timing closure.
5. To enable implementation of a complete automated physical design flow on a sample design.

Course Outcomes: Upon successful completion of this course, students will be able to:

- CO1: Develop a floorplan and power plan for a digital IC design
- CO2: Implement placement and clock tree synthesis using EDA tools
- CO3: Execute global and detailed routing while resolving congestion issues
- CO4: Analyze post-route timing reports to identify and fix setup/hold violations
- CO5: Construct a complete floorplan-to-GDSII flow for a sample design.

Course Contents

Unit I - Physical Design Fundamentals and Floor planning (09 Hours)

Physical design flow overview: netlist-to-GDSII inputs/outputs, Design partitioning, floor planning objectives (aspect ratio, utilization, core/die area), I/O planning, macro placement, pin assignment, Power planning: power ring, power straps, ring/mesh structures.

Unit II Placement (09 Hours)

Placement algorithms: global vs. detailed placement, Standard cell placement, timing-driven and congestion-driven placement, Placement legalization, Scan chain reordering during placement.

Unit III Clock Tree Synthesis (CTS) (09 Hours)

Clock tree objectives: skew, latency, insertion delay, CTS techniques: H-tree, mesh, balanced tree structures Useful skew concepts, Clock gating impact on CTS.

Unit IV Routing (09 Hours)

Global routing vs. detailed routing, Routing layers, track assignment, via optimization, Congestion analysis and fixing, special routing: clock nets, power/ground nets, differential pairs.

Unit V Timing Closure and Physical Signoff (09 Hours)

Post-route STA basics, IR drop and electro migration checks, ECO (Engineering Change Order) flow, Handoff checks: DRC/LVS at physical design stage, GDSII stream out.

Learning Resources

Text Books:

1. VLSI Physical Design: From Graph Partitioning to Timing Closure, Kahng, A.B., Lienig, J., Markov, I.L., Hu, J Springer, 2nd Edition, 2022, ISBN 78-3-030-96414-6 (hardcover) / eBook ISBN 978-90-481-9591-6
2. Static Timing Analysis for Nanometer Designs: A Practical Approach, Springer, Bhasker, J., Chadha, R. , 1st Edition, 2009, ISBN 978-0-387-93819-6 (hardcover)

Reference Books

1. Physical Design Essentials: An ASIC Design Implementation Perspective Khosrow Golshan | Springer New York | 1st Edition | 2007 | ISBN 978-0-387-36642-5
2. CMOS VLSI Design: A Circuits and Systems Perspective Neil H.E. Weste, David Money Harris | Pearson (Addison-Wesley) | 4th Edition | 2010 | ISBN 978-0-321-54774-3
3. Algorithms for VLSI Physical Design Automation Naveed A. Sherwani | Kluwer Academic Publishers | 3rd Edition | 2000 | ISBN 978-0-7923-8393-2

Recommended Certifications

1. https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ee147

Savitribai Phule Pune University **Honor Course in VLSI and Chip Design Technology**		
HVT 402 ETC - ASIC Implementation Flow Lab ,		
Teaching Scheme	**Credits**	**Examination Scheme**
Practical : 02 Hours/Week	01	Term Work: 25 Marks ,Oral : 25 Marks

Course Objectives:

1. To synthesize RTL designs and analyze resource utilization reports.
2. To perform floor planning, I/O planning, and placement using EDA tools.
3. To implement clock tree synthesis and analyze routing for digital designs.
4. To conduct post-route static timing analysis and identify timing violations.
5. To apply ECO-based fixes and achieve timing closure and design signoff.

Course Outcomes (COs):

- CO1: Perform RTL synthesis and analyze resource utilization reports
- CO2: Apply floor planning and placement techniques with I/O pin assignment
- CO3: Execute clock tree synthesis and routing while resolving DRC violations
- CO4: Analyze post-route timing reports to identify setup/hold violations
- CO5: Implement ECO-based fixes to achieve timing closure and complete design signoff.

List of Laboratory Experiments / Assignments

1. Forensics RTL synthesis and design analysis — 8-bit Carry Look-Ahead Adder (Verilog)
2. Floor planning and area constraint setup — 4-bit ALU (Verilog)
3. I/O and pin planning — 8:1 Multiplexer with 8-bit data bus (Verilog)
4. Placement and congestion analysis — 8-bit Up-Down Counter with synchronous reset (Verilog)
5. Clock tree synthesis and skew analysis — 16-bit Shift Register with multiple clock domains/enable (Verilog)
6. Global and detailed routing with DRC check — 4-bit Multiplier (Booth's algorithm, Verilog)
7. Post-route STA (setup/hold slack interpretation) — Pipelined 8-bit Adder (2-stage, Verilog)
8. Timing closure via ECO and final signoff — FSM-based Traffic Light Controller (Verilog, Moore/Mealy).

Savitribai Phule Pune University **Honor in VLSI and Chip Design Technology**		
HVT 451 ETC - Custom Layout		
Teaching Scheme	**Credits**	**Examination Scheme**
Theory : 03 Hours/Week	03	CCE : 30 Marks End-Semester: 70 Marks

Course Objectives: The course aims to:

1. To Understand the fundamentals of CMOS fabrication, layout design, and VLSI physical design flow.
2. Apply design rules and layout techniques for designing CMOS logic cells using industry-standard and open-source EDA tools.
3. Develop custom layouts for combinational and sequential circuits considering area, delay, and power optimization.
4. Perform layout verification using Design Rule Check (DRC), Layout Versus Schematic (LVS), and parasitic extraction techniques.
5. Analyze complete custom IC layouts from schematic entry to GDSII generation for fabrication readiness.

Course Outcomes: Upon successful completion of this course, students will be able to:

- CO1: Explain CMOS fabrication technology, layout principles, and physical design methodologies.
- CO2: Design custom layouts of CMOS digital circuits using standard design rules and layout techniques.
- CO3: Perform layout verification using DRC, LVS, and parasitic extraction and interpret the verification reports.
- CO4: Optimize custom layouts considering area, delay, power consumption, routing, and matching constraints.
- CO5: Design and verify complete custom VLSI blocks using open-source or commercial EDA tools and generate fabrication-ready layouts.

Course Contents

Unit I - Introduction to Custom IC Layout (09 Hours)

Introduction to VLSI Physical Design, Full Custom vs Semi Custom Design, MOS transistor structure & I-V characteristics; CMOS inverter operation, CMOS cross-section, Design hierarchy, Stick diagrams, Lambda-based design rules, Layout design methodology, Introduction to Layout Editors, GDSII database, Standard Cell Concept.

Unit II CMOS Layout Design (09 Hours)

Layout of NMOS, Layout of PMOS, CMOS Inverter, NAND gate layout, NOR gate layout, XOR implementation, Transmission Gate Layout, Multiplexer Layout, Layout optimization techniques, Sharing diffusion, Well contacts, Guard Rings.

Unit III Layout Verification (09 Hours)

Design Rule Check (DRC), Layout versus Schematic (LVS), Electrical Rule Check (ERC), Antenna Rules, Parasitic Extraction (PEX), RC extraction, Short/Open detection, Error debugging, Verification flow.

Unit IV Advanced Physical Design (09 Hours)

Cell Placement, Power Planning, Floor Planning, Routing Concepts, Clock Routing, Metal Layers, Shielding, Crosstalk, Electro migration, IR Drop, Matching Techniques, Analog Layout Basics, ESD Structures.

Unit V Applications and Custom Layout Design (09 Hours)

Introduction to OpenLane, Magic VLSI Layout Tool, Netgen LVS, KLayout, layouts: RF/analog, low-power sensor cells, datapath cells, standard cell/SRAM basics, FinFET layout, open-source flow (Magic, Sky130 PDK), DRC/LVS Implementation, GDS Generation, Tape-out Flow, Case Study of Open-source ASIC Design.

Learning Resources

Text Books:

1. Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th/5th Edition, Pearson.
2. John P. Uyemura, Introduction to VLSI Circuits and Systems, Wiley.
3. R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, 4th Edition, Wiley.

Reference Books

1. S. M. Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill.
2. Jan M. Rabaey, Digital Integrated Circuits: A Design Perspective, Pearson.
3. Christopher Saint and Judy Saint, IC Layout Basics, McGraw-Hill.
4. Mohit Arora, The Art of Analog Layout, Pearson.
5. Stephen M. Trimberger, Field-Programmable Gate Array Technology, Springer.
6. Mead and Conway, Introduction to VLSI Systems, Addison-Wesley.

Recommended Certifications

1. Google–SkyWater Open MPW Program
2. Efabless OpenLane Training
3. OpenROAD University Tutorials
4. Tiny Tapeout Design Program
5. Cadence Virtuoso Layout Design Training
6. Cadence Digital Full-Custom IC Design
7. Synopsys IC Compiler II Training
8. Siemens EDA (Mentor Graphics) Physical Design Training
9. Intel FPGA Academy (Digital Design Fundamentals)
10. VSD (VLSI System Design) – "Custom Layout" by Kunal Ghosh — stick diagrams, Euler's path, and full-custom layout using Magic (Udemy/VSD).
11. VSD – "Circuit Design and SPICE Simulations" and "Physical Design Flow using Open-Source EDA (OpenLane/Sky130 PDK)".

12. NPTEL/Swayam – "CMOS VLSI Design" (IIT faculty).
13. NPTEL/Swayam – "VLSI Physical Design" / "VLSI Design Verification and Test" (IIT/NIT faculty).
14. Coursera – "Digital VLSI Design" or "Silicon Devices and Chip Manufacturing"
15. AMD (Xilinx) FPGA Design and Implementation

Savitribai Phule Pune University **Honor in VLSI and Chip Design Technology**		
HVT 452 ETC - Physical Verification and Extraction Lab		
Teaching Scheme	**Credits**	**Examination Scheme**
Practical : 02 Hours/Week	01	Term Work : 25 Marks Oral: 25 Marks

Course Objectives: The course aims to:

1. To Understand the functionality of custom layout design tools and CMOS layout design methodology.
2. Develop custom layouts of CMOS logic gates and digital building blocks by applying lambda-based design rules.
3. Perform layout verification using Design Rule Check (DRC), Layout Versus Schematic (LVS), and parasitic extraction techniques.
4. Analyze and optimize IC layouts for area, routing, power, and performance using appropriate layout techniques.
5. Design, verify, and document complete custom VLSI layouts using open-source or industry-standard EDA tools.

Course Outcomes: Upon successful completion of this course, students will be able to:

- CO1: Create CMOS layouts for basic digital logic circuits by following standard layout design rules.
- CO2: Apply layout editing, routing, and optimization techniques to develop efficient custom IC layouts.
- CO3: Perform DRC, LVS, and parasitic extraction to verify the correctness and manufacturability of IC layouts.
- CO4: Analyze the impact of layout choices on circuit area, delay, power, and signal integrity using EDA tools.
- CO5: Design and validate a complete custom layout project from schematic to GDSII generation using open-source or commercial VLSI design tools.

List of Laboratory Experiments / Assignments

1. Installation Magic VLSI/KLayout/OpenLane, Sky130 PDK, and layout editor interface.
2. Draw the layout of a CMOS inverter, perform DRC, and verify the layout.
3. Design and verify the layouts of 2-input NAND and 2-input NOR gates using lambda-based design rules.
4. Implement and verify the layouts of XOR gate, Transmission Gate, and 2:1 Multiplexer with layout optimization techniques.
5. Perform LVS for the layouts designed in previous experiments and analyze any mismatches.
6. Extract parasitic RC parameters from the layout and compare pre-layout and post-layout simulation results using ngspice or equivalent tools.
7. Optimize the layout for reduced area, improved routing, and lower parasitic effects; analyze improvements in performance.
8. Design, verify, and document the complete custom layout of a small digital block (e.g., 4-bit Ripple

Carry Adder, 4-bit Register, 4:1 Multiplexer, or D Flip-Flop) including DRC, LVS, parasitic extraction, and GDSII generation.

Savitribai Phule Pune University		
HVT 453 ETC - Honors Projects		
Teaching Scheme	**Credits**	**Examination Scheme** ,
Theory : 04 Hours/Week	02	Term Work: 50 Marks Oral : 50 Marks

The Honors Project shall enable students to:

- Apply semiconductor and chip design concepts to solve real-world VLSI and IC design problems.
- Develop research, design, implementation, verification, and validation skills using modern EDA tools and design methodologies.
- Address emerging challenges in semiconductor technologies, advanced process nodes, low-power design, and Design for Manufacturability (DFM).
- Promote innovation, entrepreneurship, and indigenous semiconductor product development aligned with the India Semiconductor Mission.
- Encourage industry-sponsored, research-oriented, and interdisciplinary projects in VLSI, ASIC, FPGA, and semiconductor manufacturing.
- Publish research papers, patents, open-source IP cores, EDA tools, or semiconductor design frameworks.
- Enhance employability and technical competency in semiconductor design, verification, fabrication, testing, and packaging industries.

Phases of Honors Project

Capstone 1. Capstone Project – Phase I (Design and Planning)

Students shall submit a comprehensive project proposal containing:

- Problem statement
- Literature survey
- Objectives and scope
- System architecture / Block diagram
- Design methodology and workflow
- Software tools and Process Design Kit (PDK) to be used
- Technology node (e.g., SkyWater 130 nm, GF180MCU, FPGA platform)
- Expected outcomes
- Project milestones and timeline

Capstone 2. Capstone Project – Phase II (Implementation and Evaluation)

Students shall complete the project implementation and present the final demonstration.

The final evaluation shall include:

- Functional demonstration
- Design verification and validation
- Performance analysis
- Viva voce by an expert panel

Final submission shall include:

- Design files (RTL/Layout/GDSII, as applicable)
- Source code and scripts
- Simulation and verification reports
- Project report
- Presentation slides
- Demonstration video
- User manual/documentation (if applicable)

Types of Projects

The Honors Project shall belong to one or more of the following categories.

A. Research Projects

- Low-Power VLSI Design
- AI-Assisted Electronic Design Automation (EDA)
- Hardware Security and Trust
- Neuromorphic and In-Memory Computing
- Quantum and Cryogenic Semiconductor Devices
- Advanced CMOS and Beyond-CMOS Technologies
- Chiplet-Based Architectures
- 3D IC and Heterogeneous Integration

B. Design and Development Projects

- Digital ASIC Design
- Analog and Mixed-Signal IC Design
- FPGA-Based System Design
- Physical Design and RTL-to-GDSII Automation
- Custom IC Layout Design
- Standard Cell Library Development
- Verification Frameworks
- Embedded SoC Design

C. Industry-Sponsored Projects

- Industry-defined Semiconductor Design Problems
- Physical Design Automation
- DFT (Design for Testability) Implementation
- Timing Closure and Sign-off
- Process Design Kit (PDK) Development
- Silicon Validation and Characterization
- Semiconductor Packaging and Testing Solutions

D. Product Development Projects

- Commercially Viable Semiconductor IP Cores
- Open-Source EDA Tool Development

- FPGA-Based Embedded Products
- AI Accelerators and Domain-Specific Processors
- Edge AI Hardware Platforms
- Start-up Oriented Chip Design Solutions

E. Social Impact Projects

- Low-Cost Semiconductor Solutions for Education
- Healthcare and Medical Electronics ICs
- Smart Agriculture and IoT Hardware
- Energy-Efficient Embedded Systems
- Indigenous Electronics and Semiconductor Solutions under *Make in India*
- Assistive and Sustainable Electronic Systems

Savitribai Phule Pune University, Pune

Maharashtra, India

Task Force for Curriculum Design and Development

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