FACULTYOFENGINEERING

SavitribaiPhulePuneUniversity

Syllabusforthe

M.E (Electronics & Communications Engineering – VLSIDesign)

(2017Course)

(w.e.f.June2023)

Objectives

I. To serve the University, the Nation, and the Engineering profession by providing high quality educational programs to all students; engaging in research and scholarship that will extend knowledge; and assisting the economic development of the regional, state, and national economies through technology transfer.

II. To provide Post-graduate students with an excellent education through research and co-operative work experience/culture to enable successful, innovative, and life-long careers in Electronics and Telecommunication.

III. To sculpture Post-graduates students, to acquire the advanced level academic expertise and practical engineering experience necessary to function as Electronics and Telecommunication professional in a modern, ever-evolving world. Engrave Post-graduate students, to demonstrate competence by being selected for employment by industrial, academic or government entities or pursue further professional/doctoral studies.

IV. To understand the broad, social, ethical and professional issues of contemporary engineering practice. Post-graduation program will inculcate a mastery of underlying Electronics and Telecommunication Engineering and related technologies, as well as professional, ethical, and societal responsibilities.

Outcomes

a) Masters students of this program have ability to apply knowledge of mathematics, sciences and engineering to Electronics and Telecommunication problems.
b) Post graduate students gain an ability to design and conduct experiments, as well as to analyze and interpret data.
c) Learners of this program built an ability to design a system, component, devices, or process to meet desired needs.
d) Masters students of this program have an ability to function on multi-disciplinary teams and also as an individual for solving issues of Electronics and Telecommunication.
e) Learners of this program have an ability to identify, formulate, and solve Engineering problems by applying mathematical foundations, algorithmic principles, and Electronics and Telecommunication theory in the modeling and design of Electronics systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.
f) Post graduates have an ability to communicate effectively orally and in writing and also understanding of professional and ethical responsibility.
g) Develop an ability to use the techniques, skills, and modern engineering EDA tools necessary for Electronics and Telecommunication practices.
h) Learners of this program have an ability to evaluate Electronics and Telecommunication Engineering problems with cost effectiveness, features, user friendly to cater needs for product development.
i) Igniting master's students to peruse inventive concept to provide solutions to industrial, social oration problem.
j) Masters of this program generate an ability to identify, inspect, analyze, and interpret and communicate research results.
k) Post graduates recognize the need and an ability to engage in life-long learning and knowledge of contemporary issues.
l) Masters of this program put on the broad education necessary to understand the impact of Electronics and Telecommunication solutions in a global, economic, environmental, and societal prospective**.**

The following is the list of UG Courses which are eligible for taking admission in this PG Course B.E. or B. Tech in
1) Electronics & Telecommunication Engineering
2) Electronics & Communication Engineering
3) Electronics Engineering
4) IT Engineering
5) Electronics and Communication Technology
6) Computer Science Engineering
7) Computer Engineering
8) Instrumentation Engineering
9) Electrical Engineering
10) Electrical and Electronics Engineering
11) Electronics Instrumentation and Control

Syllabus Structure
M.E. (Electronics and Communications-VLSIDesign)

2017 PatternSyllabusStructure

FirstYear–SemesterI

Sr. No.	Subject Code	Subject	ExaminationScheme					Total	Credits
			Paper						
			L/P	ISA	ESA	TW	OR		
1	504701	Microelectronics & Nano- Electronics	4	50	50	-	-	100	4
2	504702	Digital IC Design	4	50	50	-	-	100	4
3	504703	Analog IC Design	4	50	50	-	-	100	4
4	504704	Research Methodology	4	50	50	-	-	100	4
5	504705	Elective I	5	50	50	-	-	100	5
6	504706	Lab Practice-I	4	-	-	50	50	100	4
		Total	**25**	**250**	**250**	**50**	**50**	**600**	**25**

ElectiveI:
1. Processor Design
2. Nanotechnology
3. Real Time Signal Processing Systems
4. Wireless Sensor Networks
5. Micro Electromechanical Systems

FirstYear–SemesterII

Sr. No.	Subject Code	Subject	ExaminationScheme					Total	Credits
			Paper						
			L/P	ISA	ESA	TW	OR		
1	504707	System-on-Programmable Chip Design	4	50	50	-	-	100	4
2	504708	Mixed Signal IC Design	4	50	50	-	-	100	4
3	504709	Design of ASICs	4	50	50	-	-	100	4
4	504710	Elective-II	5	50	50	-	-	100	5
5	504711	Lab Practice-II	4	--	---	50	50	100	4
6	504712	Seminar I	4	-	-	50	50	100	4
		Total	**25**	**200**	**200**	**100**	**100**	**600**	**25**

ElectiveII:
1. Artificial Intelligence and Soft Computing
2. Mathematical Methods and techniques for Electronics & Communication Technologists
3. High Speed ICs
4. Mixed Signal IC Design
5. Embedded Signal Processor Architecture

SecondYear– SemesterI

Sr.No.	Subject Code	Subject	ExaminationScheme					Total	Credits
			Paper						
			L/P	ISA	ESA	TW	OR		
1	604701	Testing and verification of VLSI Circuits	4	50	50	-	-	100	4
2	604702	ASIC Design	4	50	50	-	-	100	4
3	604703	Elective-III	5	50	50	-	-	100	5
4	604704	Seminar II	4	--	----	50	50	100	4
5	604705	Project Stage I	8	--	---	50	50	100	8
		Total	**25**	**150**	**150**	**100**	**100**	**500**	**25**

ElectiveIII:

ElectiveIIITopics for3 Credits
1. Value Education, Human Rights and Legislative Procedures
2. Environmental Studies
3. Renewable Energy Studies
4. Disaster Management
5. Foreign language
6. Knowledge Management
7. Economics for Engineers
8. Engineering Risk – Benefit Analysis

ElectiveIIITopics for2 Credits
1. Optimization Techniques
2. Fuzzy Mathematics
3. Design & analysis of algorithm
4. CUDA

SecondYear–SemesterII

Sr.No.	Subject Code	Subject	ExaminationScheme					Total	Credits
				Paper					
			L/P	ISA	ESA	TW	OR		
1	604706	SeminarIII	5	--	----	50	50	100	5
2	604707	ProjectStageII	20	--	---	150	50	200	20
		Total	**25**		**--**	**200**	**100**	**300**	**25**

Note: Seminar I,II & III reports should be prepared in Latex.

First Year Semester-I

504701   **MICROELECTRONICS & NANOELECTRONICS**
Credits:04

TeachingScheme: **ExaminationScheme:**

Lectures:4Hrs./week   In-Sem   :50Marks
                                                 End-Sem   :50Marks

CourseObjectives:

1. Tolearnfundamentals of Microelectronics
2. TonurturestudentsunderstandingNanotechnology
3. Tounderstandtheproperties of nano technology
4. Tolearnthenanomaterial.

CourseOutcomes:
Oncompletionofthecourse, studentwill beable to-
1. Understandthe fundamentals ofMicroelectronics
2. Understandthe fundamentals ofNanotechnology
3. Exploretheproperties of nano technology
4. Demonstratethe abilityof identification of nanomaterial

CourseContents

ModuleI:Introduction to Microelectronics(10Hrs.)
Microelectronic devices, characteristics, mathematical modeling, performance parameters, design aspects, parasitic, integration issues, layout rules, optimization techniques.

Module II: Introduction to Nanotechnology   (8 Hrs.)
Introduction to nanotechnology, the size of things, history of nanotechnology, fabrication method (top-down and bottom-up), emerging applications of nanotechnology.

Module III: Properties of Nanotechnology (12 Hrs.)
Electronic and Optical properties of nanostructures. Energy sub-bands. Electron transport in two – dimensional electron gas (density of states), Carrier scattering, resistance of a ballistic conductor, Transmission probability calculation, Electron tunneling, Resonant tunneling, Coupled Nano scale structures, and Super lattices

Module IV: Nanomaterials (12 Hrs)
Nanotechnology: Deposition techniques for Nanoscale Devices, Nanolithography, Self-Assembly Techniques, Nanomaterials, Nanoparticles, Nanowires, Nanomagnetic Materials, Nanostructure Surfaces; Instrumentation for nanoscale electronics: The 42 Atomic Force Microscope (AFM), Scanning Tunneling Microscope and scanning near field optical microscope

References:

1. NeilWesteandKamaran,"PrinciplesofCMOSVLSIDesign",EducationAsia.
2. M.Rabaey, A.Chandrakasan andB. Nikolic,DigitalIntegrated Circuits: ADesignPerspective,Pearson (Low PriceEdition)
3. CharlsRoth,"DigitalSystemDesignusingVHDL",TataMcGrawHill.
4. S-M.KangandY.Leblebici,CMOSDigitalIntegratedCircuits:AnalysisandDesign,ThirdEdition, McGraw-Hill
5. SamirPalnitkar,"VerilogHDL–AGuideto DigitalDesignandSynthesis",PHI

504702　　　　　　　　　　**DIGITAL IC DESIGN**
　　　　　　　　　　　　　　Credits:04

TeachingScheme:　　　　　　　　　　**ExaminationScheme:**

Lecture:　4Hrs./week　　　　　　　　| In-Sem | :50Marks |
| --- | --- |
| End-Sem | :50Marks |

CourseObjectives:

1. Tounderstandvarious computingarchitectures
2. Toprovidestudentsthe conceptofhandlingissuesofreconfigurecomputing
3. Toprovidestudentsimplementationapproachesof FPGAdesigninviewofreconfiguration
4. Tooutlinevariousapplicationsreconfigurecomputing

CourseOutcomes:
Oncompletionofthecourse, studentwill beable to–
1　Understandtheconceptofreconfigurablecomputinganditsintegrationoncomputingplatforms
2　Design,implementandanalyzereconfigurablesystemsintherecentapplicationdomainsusingHDL
3　UseadvancedEDAtoolstosimulateandsynthesizeHDLcodesforreconfigurablearchitectures

CourseContents

ModuleI :　Overview of VLSI　　(10 Hrs)
Overview of VLSI Design: Historical perspective, overview of VLSI design methodologies, VLSI design flow, design hierarchy, concepts of regularity, modularity, and locality, VLSI design styles, design quality, packaging technology, CAD technology.
MOS Transistor Theory: Introduction to The metal oxide semiconductor (MOS) structure, Long-channel I-V characteristics, C-V characteristics, non-linear I-V effects, DC transfer characteristics.

ModuleII : ASIC　　　　　　　　　(10 Hrs)
ASIC Design Flow: Introduction to ASIC and SoC, Overview of ASIC flow, functional verification, RTL-GATE level synthesis, synthesis optimization techniques, pre-layout timing verification, static timing analysis, floor-planning, placement and routing, extraction, post layout timing verification, extraction.
CMOS Process Technology: Fabrication process flow- basic steps, the CMOS n-Well process, layout design rules, stick diagram, full-custom mask layout design.

ModuleIII : MOS and Its Type　　　　(10 Hrs)
MOS Inverter (Static Characteristics): Resistive-load inverter, inverter with n-type 16 MOSFET load, CMOS inverter.
MOS Inverters (Switching Characteristics and Interconnects effects): Delay-time definitions, calculation of delay times, logical efforts, inverter design with delay constraints, estimation of interconnect parasitics, calculation of interconnect delay, Bus vs. Network-onChip (NoC), switching power dissipation of CMOS inverters.

ModuleIV: CMOS　　　　(10 Hrs)
Combination CMOS Logic Circuits: MOS logic circuits with depletion nMOS loads, CMOS logic circuits, complex logic circuits, CMOS transmission gates (pass gates), ratioed, dynamic and pass transistor logic circuits.
Sequential MOS logic circuits: Behaviour of bi-stable elements, SR latch circuits, clocked latch and flip-flop circuits, CMOS D-latch and edge-triggered flip-flop. Timing path, Setup time and hold time static, example of setup and hold time static, setup and hold slack, clock skew and jitter, Clock, reset and power distributions. Memory Design, SRAM, DRAM structure and implementations.

References:

1. 1. N. H. E. Weste and C. Harris, "Principles of CMOS VLSI Design: A System Perspective, 3rd Edition, Pearson Education 2007.
2. 2. CMOS Digital Integrated Circuits, Sung-Mo Kang,YusufLeblebici, 3rd edition, Tata McGrawHill, 2003
3. J. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall 2004.

504703   **Analog IC Design**
Credits:4

TeachingScheme: **ExaminationScheme:**

Lecture: 4Hrs/week   **In-Sem   :50Marks**
                                             End-Sem   :50Marks

CourseObjectives:

1. Tounderstandvariousdesignissuesinembeddedsystems
2. TolearnARM9architectureanditsprogrammingconcepts
3. TolearnembeddedLINUXoperatingsystem
4. Tomakeawareof thesignificanceof embedded networkprocessors

CourseOutcomes:

Oncompletionofthecourse, studentwill beable to–

1. Design ARMProcessorbasedEmbeddedSystems

2. Carryout programmingin Embeddedprogrammingin C, C++

3. PortLinuxoperatingsystemanddevicedrivers

4. UnderstandattributesoffunctionalunitsofNetworkProtocol

CourseContents

ModuleI : MOSFET   **(10 Hrs)**
MOSFET Operation & Model: Device Structure I/V characteristics, second order effects, Capacitances, body bias effect, DIBL, MOS small signal Models, CMOS Technology.
Basic Analog blocks: Basic concepts of amplification and biasing, Current sources and sinks, Current mirrors: Simple current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Current conveyer.

ModuleII : Amplifier   **(10 Hrs)**
Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stage with source degeneration, source follower, CG stage, Gain boosting techniques, cascode, folded cascode.

ModuleIII : Differential Amplifier   **(10 Hrs)**
Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion. Differential amplifier characterization, ICMR, Slew Rate, PSRR, offset, Frequency response of Amplifiers: Device high-frequency small-signal models; Device capacitances, ft calculation, Simplified high-frequency analysis of basic amplifiers, Miller's theorem, OCTC method for BW estimation. cascode amplifiers, differential amplifiers.

ModuleIV:Feedback & Layout   **(10 Hrs)**
Feedback Amplifier: Feedback concept, negative & positive feedback, voltage/ current, series/shunt feedback, Practical feedback circuits, Loop gain and stability, Design 14 Procedure for the feedback amplifiers.
Introduction to Layout, Fingering, Inter-digitization, Common Centroid, Process gradients, electro-migration and antenna effect.

References:

1. Design of Analog CMOS Integrated Circuits, by BehzadRazavi, McGraw-Hill
2. Analysis and Design of Analog Integrated Circuit, Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, andRobert G. Meyer, John Wiley & Sons
3. Adel S. Sedra, Kenneth C. Smith : Microelectronics Circuits, Oxford University Press
4. R. L.. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and DigitalCircuits, McGraw-Hill Education, 2010.
5. CMOS: Circuit Design, Layout, and Simulation by R. Jacob Baker, Wiley-IEEE Press(2019)

504704   **ResearchMethodology**
                          Credits:4

TeachingScheme: **ExaminationScheme:**

Lecture: 4Hrs/week   **In-Sem   :50Marks**
                                             End-Sem   :50Marks

CourseObjectives:

1. Tolearntheprocessof identificationof researchproblem
2. Tounderstandtheimportanceof statisticsinvolvedinresearch
3. Tounderstandtheprocess ofanalysisandverification ofdevelopedsystemmodel
4. Todevelop askill to prepareresearch proposals

CourseOutcomes:

Oncompletion ofthe course, studentwill beable to-

1. Outlineresearchproblem,itsscope,objectivesanderrors
2. Understandbasicinstrumentationschemesanditsdatacollectionmethods
3. Learnvariousstatisticaltechniques
4. Developmodelandcanpredicttheperformanceofexperimentalsystem
5. Writeresearchproposalsoftheirown domain

CourseContents

ModuleI :   (10 Hrs)
ResearchProblem:Meaningofresearchproblem,Sourcesofresearchproblem,Criteria/Characterist ics of a good research problem, Errors in selecting a research problem, Scope andobjectives of research problem. Basic instrumentation:Instrumentation schemes, Static anddynamic characteristics of instruments used in experimental set up, Performance under flow ormotion conditions, Data collection using a digital computer system, Linear scaling for receiverandfidelityof instrument, Role ofDSP is collected data contains noise.

ModuleII :   (10 Hrs)
Applied Statistics:Regression analysis, Parameter estimation, Multivariate statistics, Principalcomponentanalysis,Momentsandresponsecurvemethods,Statevectormachinesandunce rtaintyanalysis.

ModuleIII :   (10Hrs)
Modellingandpredictionofperformance: Settingupacomputingmodeltopredictperformance of experimental   system,   Multi-scale   modelling   and   verifying   performance ofprocesssystem,Nonlinearanalysisofsystemandasymptoticanalysis,Verifyingifassumptions hold true for a given apparatus setup, Plotting family of performance curves tostudytrendsand tendencies, Sensitivitytheoryandapplications.

ModuleIV: (10Hrs)
Developing a Research Proposal:Format of research proposal, Individual research proposal,and Institutional proposal. Proposal of a student – a presentation and assessment by a reviewcommittee consisting ofguide and external expert only. Other faculty members may attendandgivesuggestions relevant to topicof research.

References:

1. MelvilleStuart,GoddardWayne,"Researchmethodology:AnIntroductionforScience &Engineeringstudents".
2. RanjitKumar,"ResearchMethodology:AStepbyStepGuideforBeginners",Secondedition.
3. Dr.KothariCR,"ResearchMethodology:MethodsandTrends".
4. Dr.SharmaSD,KedarNath,"OperationalResearch".

LaboratoryAssignments/Experiments:

1. Designatypicalresearchproblemusingscientific method.
2. Design adata collection systemusingdigitalcomputersystem.
3. Studythevarious analysis techniques.
4. Designanddevelopacomputingmodeltopredicttheperformanceofexperimentalsystem.
5. Developthefollowingresearch proposal:A. IndividualB. Institutional.

504705-1   **ProcessorDesign(ElectiveI)**
                          Credits:5

TeachingScheme: **ExaminationScheme:**

Lecture: 4Hrs/week   In-Sem   :50Marks
                          End-Sem   :50Marks

CourseObjectives:
1. Tolearnarchitecturefundamentalsofprocessordesign
2. TounderstandmemorymanagementofCISCandRISCprocessors
3. Togainknowledgeof architectureanddesignissuesinDSP
4. Toupdatetheinformationwithrespecttoruntimere-configurable processors

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-
1. VisualizeprobableProblems,fallacies andPitfallsinProcessorDesign
2. UnderstandExtremeCISCandRISC,VeryLongInstructionWord(VLIW),overlyaggressivepipelining,unbalanced processor
3. GainskillstoimplementProcessor functionalcomponentslikeMAC

CourseContents

ModuleI :   **(10 Hrs)**
EmbeddedComputerArchitectureFundamentals:Componentsofanembeddedcomputer,Architectureorganization,waysofparallelism,I/Ooperationsandperipherals.Problems,Fallacies,   and Pitfalls in Processor Design for a high level computer instruction set architectureto support a specific language or language domain, use of intermediate ISAs to allow a simplemachinetoemulateit'sbetters,stackmachines,overlyaggressivepipelining,unbalancedprocessor design, Omitting pipeline interlocks, Non-power-of-2 data-word widths for general-purposecomputing.

ModuleII :   **(10 Hrs)**
Memory:Organization,Memorysegmentation,Multithreading,Symmetricmultiprocessing.ProcessorDesignFlow:Capturingrequirements,Instructioncoding,Explorationofarchitectureorganizations, hardwareandsoftwaredevelopment.ExtremeCISCandextremeRISC,Verylonginstruction   word (VLIW).

ModuleIII :   **(10Hrs)**
Digital Signal Processor: Digital signal processor and its design issues, evolving architecture ofDSP, nextgeneration DSP. Customizable processors: Customizable processors and processorcustomization, A benefit analysis ofprocessor customization, use of microprocessor cores inSOCdesign, benefits ofmicroprocessor extensibility.

ModuleIV: **(10 Hrs)**
Run time Re-configurable Processors:Run time Re-configurable Processors,Embedded micro-processortrends,instructionsetmetamorphosis,reconfigurablecomputing,run-timereconfigurableinstructionsetprocessors,coarsegrainreconfigurableprocessors.ProcessorClock Generation and Distribution: Clock parameters and trends, Clock distributionnetworks,de-skewcircuits,jitterreductiontechniques,lowpowerclockdistribution.AsynchronousProcessor Design: Asynchronous and self-timed processor design, need of asynchronousdesign,developmentofasynchronousprocessors,asynchronousdesignstyles,features of
asynchronousdesign.

References :

1. NurmiJari,"ProcessorDesign-SystemonChipComputingforASIC"sandFPGA",SpringerPublications.
2. FrantzG,"TheDSPandIts ImpactontheTechnology".
3. LeibsonS,Tensilica,"CustomizableProcessorsandProcessorCustomization".
4. CampiF,"Run-TimeReconfigurableProcessors".
5. GarsideJ,FurberS,"AsynchronousandSelf-TimedProcessorDesign".
6. RusuS,"ProcessorClockGenerationandDistribution".
7. DehonAndre,"ReconfigurableArchitectureforGeneralpurposeComputing".

LaboratoryAssignments/Experiments:

1. Design andimplementMACUnitonPLD
2. Design andimplementCPUonPLD
3. Design and implementCarrylook-aheadgeneratoronPLD
4. Design andimplementationofTranslationlook-asidebuffer.

504705-2 **NANOTECHNOLOGY(ElectiveI)**
Credits:5

TeachingScheme: **ExaminationScheme:**

Lecture: 4Hrs/week   **In-Sem :50Marks**
                                            End-Sem :50Marks

CourseObjectives:

1. Toget familiar withfundamental sciencebehindNano technologyandsystems
2. Toacquirebasicunderstandingof materialsciencefordesigningNEMS basedsystems
3. Tounderstandtheprincipleofbiomaterialandtheir applicationstoBio-medicalsystems

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-
1. Choosesuitablematerialbasedonthe propertiesfor Nanotechnology
2. Learntechniquesofnano-structuresandfabrication
3. GainknowledgeofdesigninganddevelopingNEMSbasedsystems

CourseContents

ModuleI :   **(10 Hrs)**
Thefundamentalsciencebehindnanotechnology,biosystems,molecularrecognition,quantummechanics&quantumideas,optics.Smartmaterials&Sensors,self-healingstructures,heterogeneousnano-structures&composites,encapsulations,naturalnano-scalesensors,electromagneticsensors, biosensors,electronicnoses.

ModuleII :   **(10Hrs)**
Nanostructures,Micro/Nano-devices,   nano-materialsSynthesisandApplications,Molecule-BasedDevices.-IntroductiontoCarbonnano-tubes.-nano-wires.-
IntroductiontoMicro/Nanofabrication.-StampingTechniques.Methods and Applications.

ModuleIII :   **(10Hrs)**
Materials Aspects of Micro- and Nanoelectromechanical Systems,- MEMS/NEMS , Devices andApplications.Nanostructuredevices–Resonanttunnelingdiodes,Field-effecttransistors,Single-electrode transfer devices. Scanning Probe Microscopy,Noncontact Atomic ForceMicroscopy.

ModuleIV(10Hrs)
LowTemperatureScanningProbeMicroscopy,DynamicForce Microscopy.-
.Nanolithography,Lithographyusingphotons,electron beams softlithography.Bio-medical applications.

References:
1. Springer Handbookof Nanotechnology
2. Rattner Mark , Rattner Daniel, "Nanotechnology: A Gentle Introduction to the Next BigIdea"
3. KulkarniSulbhaK,"Nanotechnology:Principals&Practices",CapitalPublications
4. VlaimirMitin,"Introductiontonanoelectronicsscience,Nanotechnology,EngineeringandApplications",CambridgeUniversityPress

LaboratoryAssignments/Experiments:

1   IntroductionofanalysisandcharacterizationofNanostructuredmaterials,coatingandthinfilm sensors.
2   SurfacetensionmeasurementofNanofluids.
3   Toobservesizeand slopeof theNano sized sampleusingscanningelectron microscopy.
4   Design,simulationandanalysisofNanostructures.

504705-3   Real Time Signal Processing (Elective I)
Credits: 5

TeachingScheme:	ExaminationScheme:	
Lecture: 4Hrs./week	In-Sem	:50Marks
	End-Sem	:50Marks

CourseObjectives:
1. Toprovidedetailunderstandingof MOSdevices' structuresandoperations
2. TounderstandtheeffectofvariousmaterialsonthecharacteristicsofMOSFET
3. Toacquaintthestudents with SPICEtoolformodelingoftransistorbehavior
4. ToprovideabriefknowledgeofAdvancedMOSFETmodels

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-
1   AnalyzeMOSFETmodels
2   LearnMOSFETcharacterizationusingSPICEsimulation
3   GaininformationaboutadvancedMOSFETmodels
4   Understandnon-classical MOSstructures

CourseContents

ModuleI :   (10 Hrs)
The Discrete Fourier Transforms Discrete Fourier transform, properties of DFT. Frequency domain sampling, Frequency analysis of signals using the DFT. DFT of discrete time signals, Relation between DFT and Z-transform. IDFT.

ModuleII :   (10 Hrs)
Fast Fourier Transforms
Direct computation of DFT, Need of efficient computation of DFT, Radix-2 Decimation in time domain and decimation in frequency domain algorithms (DIT- FFT and DIF-FFT), Linear filtering methods based on DFT Goertzel Algorithms

ModuleIII :   (10 Hrs)
Implementation of Discrete time systems FIR Systems- Direct Form-I, Direct Form-II, Cascade, Parallel structure IIR Systems- Direct Form, Cascade, Linear phase structure, Frequency sampling Structure.

ModuleIV: (10Hrs)
Design of IIR and FIR filters, Design of digital IIR digital filters from analog filters, Impulse invariance method and bilinear transformation method. Frequency transformations. Design of digital FIR filters using window method.

References:

1. YannisTsividis,"Operationandmodelingofthe MOStransistor",Oxford UniversityPress.
2. KangS.M,"CMOSDigital IntegratedCircuits", TataMc-GrawHill.
3. CarlosGalup&Montoro,
   "MOSFETModelingforCircuitAnalysisandDesign",WorldScientific.
4. DonaldNeamen,"SemiconductorsPhysicsandDevices",TataMc-Graw Hill.
5. SzeS.M,"PhysicsofSemiconductor Devices,SecondEdition, WileyPublications.

504705-4   WirelessSensorNetwork(ElectiveI)
Credits:5

TeachingScheme: **ExaminationScheme:**

Lecture: 4Hrs./week   **In-Sem   :50Marks**
                                                        End-Sem   :50Marks

CourseObjectives:
1. Tounderstand basicWSN Technologyandits supportingProtocols
2. Tolearnroutingprotocolsand theirdesignissuesinWSN
3. Tounderstandsensor-management,sensor-networkmiddleware andoperatingsystems
4. TounderstandWSNlayers'issues andtheirprotocols

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-

1   GainknowledgeofArchitectureofWSNnetwork
2   UnderstandPhysical,DatalinkandNetworklayer aspectswiththeirprotocols
3   Learndifferenttechniquesofpowermanagementandsecurity
4   Exhibittheknowledgeof operatingsystemsinWSNsystems

CourseContents

ModuleI :   **(10Hrs)**
Introduction: Motivation for a Network of Wireless Sensor Nodes, Sensing and
SensorsWirelessNetworks,ChallengesandConstraints.Applicationsto:Healthcare,Agricult
ure,Trafficand others.

ModuleII :   **(10 Hrs)**
Architectures: Node Architecture; the sensing subsystem, processor subsystem,
communicationinterface, LMote, XYZ, Hogthrob node architectures. Power Management -
Through localpower, processor, communication subsystems and other means, time
Synchronization need,challenges and solutions overview for ranging techniques. Security
Fundamentals, challengesandattacks ofNetworkSecurity, protocolmechanisms forsecurity.

ModuleIII :   **(10 Hrs)**
OperatingSystems-FunctionalandnonfunctionalAspects,shortoverviewofprototypes–
TinyOS,SOS, Contiki, LiteOS,Sensor grid.

ModuleIV: **(10 Hrs)**
Physical Layer- Basic Components, Source Encoding, Channel Encoding, Modulation,
SignalPropagation.MediumAccessControl–
types,protocols,standardsandcharacteristics,challengesNetworkLayer-RoutingMetrics,
differentroutingtechniques.

References:
1. DargieW.,PoellabauerC.,"Fundamentalsofwirelesssensornetworks:theoryandpractice",
   John Wileyand Sons

2. SohrabyK.,Minol,D.,ZnatiT.,"Wirelesssensornetworks:technology,protocols,andapplicatio
   ns",John Wileyand Sons

3. HartJ.K.,MartinezK.,"EnvironmentalSensorNetworks:Arevolutionin
   theearthsystemscience",Earth-ScienceReviews.

4. FengZhao,LeonidasJ.Guibas,"WirelessSensorNetworks:AnInformationProcessingApproac
   h".

LaboratoryAssignments/Experiments:

1. Readingdatafrom Sensornode.
2. Implement50stationarynodestopologyusingNS2fordatatransmissionandrecordQoSparameter softhe Networks/ Test bed.
3. Implement50dynamicnodestopologyusingNS2fordatatransmissionandrecordQoSparameters ofthe Networks /Test bed.
4. OnanyabovetopologychangetheNetworklayer/Transportlayer/MAClayerprotocolandmonito rthechanges between anytwo protocols/ test bed usingNetworkSimulator.

504705-5   Micro Electromechanical Systems (ElectiveI)
Credits:5

TeachingScheme: **ExaminationScheme:**

Lecture: 4Hrs/week   In-Sem   :50Marks
                                                       End-Sem   :50Marks

CourseObjectives:
5. Toprovidedetailunderstandingof MOSdevices' structuresandoperations
6. TounderstandtheeffectofvariousmaterialsonthecharacteristicsofMOSFET
7. ToacquaintthestudentswithSPICEtoolformodelingoftransistorbehavior
8. ToprovideabriefknowledgeofAdvancedMOSFETmodels

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-
5   AnalyzeMOSFETmodels
6   LearnMOSFETcharacterizationusingSPICEsimulation
7   GaininformationaboutadvancedMOSFETmodels
8   Understandnon-classical MOSstructures

CourseContents

ModuleI :   (10 Hrs)
Micro fabrication: Micro fabrication introduction and overview: Material for fabrication, Fabrication equipment, Growth technology, Silicon-based process.
Fabrication technology:
Pattern transfer technology, Lithography– photolithography, Resist technology, Micromachining– wet etch and dry etch Materials processing technology: Material deposition methods, Basic ion implantation and diffusion doping process, Low and high temperature process, Device packaging methods Characterization technology for micro fabrication process, Design criteria and fabrication method for micro device applications, Micro fabrication process integration.

ModuleII :   (10 Hrs)
Introduction to MEMS: Magnetic Sensors, Piezoresistive MEMS , Pressure Sensors, Thick-film and Piezo MEMS, MEMS Actuators, MEMS resonant sensors, Measurement systems, Physical sensors, Modeling the dynamics of sensor systems, Intelligent sensors, Thermal sensors, Charge amplifiers. Microfluidics : Principles of miniaturization, scaling laws, Theory of Microfluidics
and Nano fluidics , The diffusion of molecules and micro scale mixing, Technological
production of components: mixers and pumps.

ModuleIII :   (10 Hrs)
MEMS Sensors and Actuators: Sensing and Actuation: Introduction, Piezoresistive and Capacitive sensing. Electrostatic actuation, Pressure sensors, Accelerometers, Gyroscopes. Interfacing with Sensors and Actuators: Bridge circuits, Amplifiers, Filtering and signal conditioning. RF MEMS: Tunable capacitors, Inductors on chip, Resonators, Mechanical filters, MEMS for mobile phones On-a-chip.

ModuleIV: (10Hrs)
Practical Applications of MEMS:Applications of Sensors in Industry, Sensor Performance,
Sensor Packaging, 3D printing/rapid prototyping, Design of sensor and packaging,
Simulation of physical process, Simulation of electrical interface and behavior, Construction
of package, Construction of sensor, Testing, Technical reporting of results.

References:

1. Beeby S P, Ensell Graham, Michael Kraft and Neil White, "MEMS MechanicalSensors"Artech House Publications, ISBN-10: 1580535364 /ISBN-13: 978-1580535366.
2. Kovacs, "Micro machined Transducers Sourcebook", McGraw-Hill Publications, ISBN-10:0072907223/ISBN-13:978-0072907223.
3. Gardner W, Varadan V K &Awadelkarim O O," Microsensors, MEMS and Smart Devices:
4. Technology, Applications and Devices", Julian Publications, ISBN-10: 047186109X/ISBN13: 978-0471861096.
5. Kaajakari Ville," Practical MEMS: Analysis and Design of Microsystems", ISBN-10:9780982299104, ISBN-13: 978-0982299104.
6. MalufNadim,WilliamsKirt, " An Introduction to Microelectromechanical SystemsEngineering", John Willy & sons Ltd.ISBN-10: 1580535909/ ISBN-13: 978-1580535908.
7. Mohamed Gad-el-Hak," The MEMS Handbook", Second Edition , 3 Volume Set.
8. Stephen D. Senturia," Microsystem Design", Second edition.

504706   **Lab Practice I**
                              Credits:4

TeachingScheme: **ExaminationScheme:**
Lectures: 4Hrs/week   TW   :50 Marks
                                             OR   :50Marks

Group A (Any 3 from following list)

1. To design, prepare layout and simulate CMOS Inverter for the given specifications of loadcapacitance,propagationdelay, powerdissipation, foundryetc.

2. To design logic for ATM machine password and accessfunctionality.Assume suitableI/Os such as card sense, 4 digit PIN number, type of account, amount, other facilitiesneededetc.

3. TodesignCMOSlogicforF=A+B(C+D)+EFGandpreparelayout.Assumesuitablecapacitiveload &foundry.MeasureT_R,T_F&T_{PD}.

4. To draw FSM diagram, write HDL code, synthesis, simulate, place & route for Tea/Coffeevending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense,pourvalve, timer count,alarmetc. You mayassumeadditionalI/Os too.

5. To design and simulate combinational logic to demonstrate hazards. Also, simulatethe samelogicredesigned for removal ofhazards.

Group B (Any 2 from following list)

1   To design and implement a Multi Context (4) 4-LUT and implement using HDL and download on FPGA.
2   Top level modular and hierarchical designs of Adder and Subtractor such that they can be replaced.
3   An adaptive design of LED shifter (Right & Left shift)
4   SoPC based Hw-SW design (Soft/Hard Processor + FPGA HW)

Group C (Any 3 from following list)

1   Write a program for 4*4 Matrix Keypad Interface.
2   To develop character device driver for GPIO
3   One experiment based on any one of development Platform: Arduino, Beaglebon, Rasberry Pi, Intel Galileo Gen 2.
4   Interfacing USB & CAN of LPC 1768.
5   Write a program for External Interrupt.

504707   **System-on-Programmable Chip Design**
Credits:4

TeachingScheme:	**ExaminationScheme:**	
Lectures: 4Hrs/week	**In-Sem**	**:50Marks**
	End-Sem	**:50Marks**

CourseObjectives:
1. Tounderstand theoryofanalogcircuitsusingMOS small signalmodels
2. Tounderstanddesignprinciplesandtechniques of CMOSAmplifiers
3. Togaindesignaspectsof HFandLowNoiseAmplifiers
4. Tolearn differentmethods of Stabilityand FrequencyCompensation

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-
1. UnderstanddesignconceptsandissuesofCMOSamplifiers
2. LearndifferentCompensationtechniques
3. Acquiretheknowledgeofdesigningof HFandLowNoiseAmplifiers

CourseContents

ModuleI :   (10Hrs)
Driving Forces for SoC - Components of SoC - Design flow of SoC - Hardware/Software nature of SoC - Design Trade-offs - SoC Applications, Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), Elements in Instruction Handling- Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom- Designed processors- on-chip memory.

ModuleII :   (10Hrs)
On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, Core Connect, Wishbone, Avalon - Network- on chip: Architecture-topologies-switching strategies - routing algorithms -low control, Quality-of-Service- Configurability in communication
Architectures.

ModuleIII :   (10 Hrs)
Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse - IP integration - IP evaluation on FPGA prototypes.

ModuleIV: (10Hrs)
Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design. Manufacturing test of SoC: Core layer, system layer, application layer- P1500 Wrapper Standardization-SoC Test Automation (STAT).

References:
1. Michael J.Flynn, Wayne Luk, "Computer system Design: System on-Chip", Wiley-India, 2012
2. Sudeep Pasricha, Nikil Dutt, "On Chip Communication Architectures: System on ChipInterconnect", Morgan Kaufmann Publishers, 2008.
3. W.H.Wolf, "Computers as Components: Principles of Embedded Computing System.

LaboratoryAssignments/Experiments:

1. To design cascode current mirror for output current of 100 µA. Prepare layout and simulate.Commenton output resistance.
2. To design, prepare layout and simulate CMOS differential amplifier for CMRR of 40 dB.CommentonICMR.
3. To design, prepare layout and simulate multistage CMOS RF amplifier in 90 nm technologyforvoltagegainof 60dB, bandwidthof 100MHz, and sourceimpedanceof 50 Ω.
4. To design CMOS RF amplifier for voltage gain of 60 dB. Suggest and design suitabletechnique to enhance the bandwidth. Simulate each added technique step by step. Commentontheimprovementresulted eachtime.Preparelayout ofthe finalschematicandsimulate.
5. List the sources of cross talk. Explore in detail, the existence of cross talk in each case.Explain the mitigation techniques. Prepare case study for one of them. Verify the cross talkandits mitigation through simulation.

504708   **SystemonChip**

Credits:4

TeachingScheme: **ExaminationScheme:**

Lecture: 4Hrs/week   **In-Sem   :50Marks**
                                                   End-Sem   :50Marks

CourseObjectives:
1. Tounderstand thebasicconcepts and models inSoC
2. ToexploreMicro-programmedArchitecturesandSoCmodeling
3. Toexplorefeaturesof simulationand synthesisofRTLintent
4. Tolearnrecenttrendsin SoCdesign

CourseOutcomes:
Oncompletionofthecourse, studentwill beable to–
1. LearnDesignflow graphsandflowmodeling
2. UnderstandSoCmodelingandinterfacing
3. GainknowledgeofSoCmemorysystemdesign,embeddedsoftwareandenergymanagementtec hniquesforSoCdesign,SoCprototyping,verification,testingandphysicaldesign
4. Design, implementand test SoC

CourseContents

ModuleI :   **(10 Hrs)**
Basic Concepts: The nature of hardware and software, data flow modelling and implementation,theneedforconcurrentmodels,analyzingsynchronousdataflowgraphs,controlflow modelling and the limitations of data flow models, software and hardware implementation ofdata flow, analysis of control flow and data flow, Finite State Machine with data-path, cyclebased bit parallel hardware, hardware model, FSMD data-path, simulation and RTL synthesis,languagemappingfor FSMD.

ModuleII :   **(10 Hrs)**
Micro-programmedArchitectures:limitationsofFSM,Micro-programmed:control,encoding ,data-path,Micro-programmedmachineimplementation,handlingMicro-programinterruptand pipelining , General purpose embedded cores , processors, The RISC pipeline, programorganization,analyzingthequalityofcompiledcode,SystemonChip,concept,designprincipl es,portablemultimediasystem,SOCmodelling,hardware/softwareinterfaces,synchronizationsche mes,memorymappedInterfaces,coprocessorinterfaces,coprocessorcontrolshelldesign, data and control design, Programmer'smodel .

ModuleIII :   **(10 Hrs)**
RTLintent:Simulationrace,simulation-synthesismismatch,timinganalysis,timingparameters   for digital logic, factors affecting delay and slew, sequential arcs, clock domaincrossing ,bus synchronization , preventing data loss through FIFO, Importance of low power,causes and factors affecting power, switching activity, simulation limitation, implication onsynthesisand on backend.

ModuleIV: **(10Hrs)**
ResearchtopicsinSOCdesign:ASOCcontrollerfordigitalstillcamera,multimediaIPdevelopment image and video CODECS, SoC memory system design, embedded software, andenergy management techniques for SOC design, SOCprototyping, verification, testing andphysicaldesign.

References:

1. PatrickR.Schaumont,"APracticalIntroductiontoHardware/SoftwareCo-design",SpringerPublications.
2. SanjayChuriwala,SapanGarg,"PrinciplesofVLSIRTLDesignAPracticalGuide",SpringerPublications.
3. Youn-LongSteveLin,"EssentialIssuesinSOCDesign,DesigningComplexSystems-on-Chip",SpringerPublications.
4. WayneWolf,"ModernVLSIDesignSystemsonChip",PearsonEducation.
5. RajanishK.Kamat,SanthoshA.Shinde,VinodG.Shelake,"UnleashtheSystemOnChipusingFPGAsand HandelC", Springer Publications.

LaboratoryAssignments/Experiments:

1. Design, simulate and implement FSM on PLD for detection of either of inputsequence X=…1001. or…1101…sequenceandsetoutputflagsY ="1"or Z="1" respectively. What is effect on area, speed, fan out and power by implementingthisdesign usingdifferent state encodingstyles?

2. Design and implement MOD4 counter on PLD and verify multi-clock operations byprobinglogic analyzer

Control bits	Countupdateafter everysec.
00	0.25sec
01	0.5sec
10	1sec
11	4sec

Why gated clock is not preferred in digital design? Write Verilog code to implement CMOSlayoutwhich willgenerateglitch alsodesignaRTLbyWriteVHDLwillgenerate glitch andalsomeasureit usingelectronictest equipment.

3. Implement temperature logging system as a co-design by Interfacing FPGA &μC8051as follows :

   i)   LM35interfaced withADC
   ii) ADCinterfacedwithFPGA
   iii) FPGAinterfaced withμC8051
   iv) μC8051isinterfacedwith LCD

4. To display real-time room temperature. If temperature is greater than 250 C Bi-colorsLEDshouldchangeits normal

   Greencolor to RED color via opto-isolator byactuation of relay

504709   **EmbeddedAutomotiveSystems**
Credits:4

TeachingScheme: **ExaminationScheme:**

Lecture: **4Hrs/week**   **In-Sem**   **:50Marks**
                                                   End-Sem   **:50Marks**

CourseObjectives:

1. Tointroducethe potential of automotivesystems in industries
2. Tounderstand Automotive SensorySystems
3. Toexplaintheimportanceof Automotivecontrolinsystemdesign
4. Tomakestudentawareof differentAutomotiveprotocols forinternal communication

CourseOutcomes:
Oncompletionofthecourse, studentwill beable to-

1. Understandthe fundamentalsofdifferentAutomotiveSystems
2. Learnutilityof sensorsand instrumentationin vehiclesystems
3. Designcontrolsystemforvariousvehicularmodules
4. Acquireknowledgeofvarious automotiveprotocols
5. Providetechnical embedded solutionsforthedevelopmentof automotiveSystems

CourseContents

ModuleI :   **(10 Hrs)**
AutomotiveSystemsOverview:AutomotiveVehicleTechnology,OverviewofVehicleCategories,
Various Vehicle Sub Systems like Chassis, Body, Driveline, Engine technology,Fuellingtechnology,vehicleEmission,Brakes,Suspension,Emission,Doors,Dashboardi nstruments, Wiring Harness, Safety & Security , Comfort & Infotainment, Communication &Lighting, FutureTrendsinAutomotiveEmbeddedSystems:HybridVehicles,ElectricVehicles.

ModuleII :   **(10Hrs)**
Automotive Sensory System :Automotive Sensorsand Transducers: Temperature, Manifold andBarometric Pressures, Humidity, Carbon Dioxide (CO2),Carbon Monoxide (CO), Oxygen (O2)Sensor, Proximity Distance Sensors, Engine Speed sensor, Throttle Position Sensor, PressureSensors, Knock Sensor & Mass Flow Sensor. Typical Sensors Specifications & MicrocontrollerInterfaceConsiderations, Sensor Calibration, Curvefitting.

ModuleIII :   **(10Hrs)**
Automotive Control System Design:Digital Engine Control, Features, Control Modes for FuelControl,Discrete TimeIdle SpeedControl,EGRControl,Variable Valve Timing Control,Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes,Cruise Control System, Cruise Control Electronics, Anti-locking Braking System, ElectronicSuspensionSystem, ElectronicSteeringControl, Four-WheelSteering.

ModuleIV: **(10 Hrs)**
AutomotiveProtocols:TheneedforProtocol,AutomotiveProtocols:LIN,CAN,KWP2000&J1939,Fl exRay,Test,CalibrationandDiagnosticstoolsfornetworkingofelectronicsystems likeECUSoftwareandTestingTools,ECUCalibrationTools,VehicleNetworkSimulation.AdvancedTr ends in AutomotiveElectronics:AUTOSAR Architecture.

References:

1. WilliamB.Ribbens,"UnderstandingAutomotiveElectronics-AnEngineeringPerspective",Seventhedition, Butterworth-HeinemannPublications.
2. RonaldK.Jurgen,"AutomotiveElectronicsHandbook",Mc-GrawHill.
3. Kiencke,Uwe,Nielsen&Lars,"AutomotiveControlSystemsforEngine,DrivelineandVehicle",Second edition, Springer Publication.
4. Tao Zhang, Luca Delgrossi, "Vehicle Safety Communications: Protocols, Security andPrivacy",WileyPublication.
5. RobertBosch,"AutomotiveHand Book",Fifthedition,SAEPublications.

LaboratoryAssignments/Experiments:
1. WriteaprogramforSensingEngineSpeed,LoadandTemperature.
2. Developatransistorized IgnitionDriver.
3. Design asinglecylinderengineManagementSystem.
4. Perform a case studyfor anytwo automotive protocols.
5. StudythefunctionaldesignaspectsofHybridAutomotiveSystems.

504710-1   **EmbeddedProductDesign(ElectiveII)**
Credits:5

TeachingScheme: **ExaminationScheme:**

Lecture: **4Hrs/week**   **In-Sem**   **:50Marks**
                                             End-Sem   **:50Marks**

CourseObjectives:
1. Tounderstanddesignchallengesof embeddedhardwareandsoftware
2. Togainknowledgeoftestingandverification issuesindesigncycle
3. Tointroduceh/wand s/w design models withdifferent technology
4. Tolearn theimportance ofdocumentationfortechnologytransfer

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-
1. Learnspecificationsanddesignchallenges ofembeddedproducts
2. Estimatecostofembeddedproduct
3. UnderstandtheaspectsofMechanicalPackaging, Testing,reliabilityand failureanalysis,EMI/RFICertification and
 Documentation
4. Demonstratetheknowledgeofembeddedproductdesignrelatedhardwareandsoftwaredesigntools

CourseContents

ModuleI: **(10Hrs)**
Overview of Embedded Products: Need, Design challenges, product survey, specificationsofproduct need of hardware and software, Partitioning of the design into its software andhardwarecomponents,Iterationand refinement ofthepartitioning.
ModuleII: **(10Hrs)**
DeignModelsandTechniques:variousmodelsofdevelopmentofhardwareandsoftware,theirfeatures,differentProcessor technology,ICtechnology,Design Technology.
ModuleIII: **(10Hrs)**
Modules of Hardware and Software:Tradeoffs, Custom Single-purpose processors, General-purposeprocessors,Software,Memory,Interfacing,Designtechnology-Hardwaredesign,FPGAdesign,firmwaredesign,driverdevelopment,RTOSporting,costreduction,re-engineering,optimization,maintenance,validationanddevelopment,prototyping,turnkeyproductdesign.
ModuleIV: **(10Hrs)**
Testingandverification:Embeddedproducts-areasoftechnology,Designandverification,Integration of the hardware and software components, testing- different tools, theirselectioncriterion. Certification and documentation: Mechanical Packaging, Testing, reliabilityand failureanalysis, communication protocols, Certification (EMI/ RFI) and its documentation.Studyof anytwo real life embedded products in detail.

References:
1   VahidFrankand Tony Givargis , "Embedded System Design: A UnifiedHardware/SoftwareIntroduction", JohnWileyPublication.
2   MarwedelP,"EmbeddedSystemDesign",SpringerPublication.

LaboratoryAssignments/Experiments:
1. Toestimatetechno-commercialfeasibilityofanyoneembeddedproductsuchasmobilephone,programmablecalculator,tablet PC, biometricssystem, set topboxetc.
2. To studydesignconsiderationsof anyoneembeddedproducte.g.laptop,videoconferencingsystem,surveillance/ securitysystem, EMG/ECGmachine etc.
3. To designanyoneembedded productto solveanyreal lifeproblems.
4. Totest thehardwaredesignedforaboveassignment (3)usingsuitablesimulation tool.
5. Tosimulatethesoftwaredesignedfortheaboveassignment(3)usingsuitablesimulationtool.

504710- **HighSpeedICs (ElectiveII)**
Credits:5

TeachingScheme: **ExaminationScheme:**

Lecture:4Hrs/week **In-Sem :50Marks**
End-Sem :50Marks

CourseObjectives:
1. Tounderstandbasicdesignaspectsofhighfrequencycircuits
2. Toexplaindifferent characteristicsofhighspeedlogicfamilies
3. Tolearndesignissuesof interconnectsinHighSpeedCircuitDesign

CourseOutcomes:
Oncompletionofthecourse, studentwill beable to–
1. AcquireknowledgeaboutHighSpeedVLSICircuitsDesign
2. Identifythebasicneedof highspeeddigitallogicfamilies
3. Understandvarioustypes VLSIinterconnections
4. Analyzevariousinterconnection delaymodels
5. Acquireinsightsofnanotechnologycircuitsinterconnections

CourseContents

ModuleI : **(10Hrs)**
Abriefhistoryofhigh-frequencyintegratedcircuitsanditsdesign,High-
frequencycircuitsinwireless,fiber-opticand imagingsystems.
ModuleII : **(10 Hrs)**
High-speed digital logic families,Design methodology for maximum data rate,Bi-CMOSMOS-
HBT logic,Pseudo-CML logic, Other bipolar, MOS and Bi-CMOS CML, and
ECLgates,CML/ECLgate layout techniques.
ModuleIII : **(10Hrs)**
Metal-Insulator-
SemiconductorMicrostripLineModelofanInterconnection.,TransmissionLineAnalysisofSingleLe
velInterconnections,TransmissionLineAnalysisofParallelMultilevelInterconnections,Very
HighFrequencyLossesinaMicrostripInterconnection,CompactExpressionsforInterconnectionDela
ys,InterconnectionDelaysinMultilayerIntegratedCircuits
ModuleIV: **(10Hrs)**
High Speed Circuit Design:High Speed Properties of logic gates-power, speed and
packaging.Cross talk in solid ground and slotted ground planes, Near end and Far end cross talk.
Endterminators and cross talk in terminators, Vias and its characteristics. Stable voltage
references,Connectors andcross talkdue toconnectors. Clock jitter and signalintegrity
mechanismforhighspeed link. Clock and power distribution relatedproblems.
References:
1. VoinigescuSorin,"High-FrequencyIntegratedCircuits",CambridgeUniversityPress.
2. GoelAK,"High-SpeedVLSIInterconnections",Secondedition,Wiley-IEEEPress.
3. NakhlaMS,ZhangOJ,"ModelingandSimulationofHighSpeedVLSIInterconnects",Springe
rPublication.
4. Ludwig Reinhold, BretchkoPavel, "RF Circuit Design Theory and
Applications",Pearsoneducation.
5. HowardJohnson,GrahamMartin,"HighSpeeddigitalDesign-
AHandbookofBlackMagic",Pearson education.

LaboratoryAssignments:
1. SimulateRCcircuitandcommentontransientresponse.
2. SimulatestartupmodelofRLC.
3. SimulateatransmissionlinetoevaluateVSWR,reflectioncoefficientparametersconsideringdifferent loadingconsiderations using analogsimulation tool.
4. Plotstabilitycircle,forgiven valuesofSparameters.

504710-3   **MixedSignalICDesign(ElectiveII)**
                              Credits:5

TeachingScheme: **ExaminationScheme:**

Lectures: 4Hrs/week   **In-Sem   :50Marks**
                                           End-Sem   :50Marks

CourseObjectives:
1. TointroducedMixedSignallayoutissuesincircuitdesign
2. ToexplaintheArchitecturesofADCandDAC
3. ToacquireknowledgeonModelingDataConvertors

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-

1. Understandthemixedsignalissuesin circuitdesign
2. LearnmodelingdifferentADCandDAC
3. Applymethodsto improve SNR
4. Exploretheoperationof delta-sigma/sigma-deltaconverterandtheirissues

CourseContents

ModuleI :   **(10Hrs)**
Analog versus discrete time signals, Converting analog signal to digitalsignal, Sample andhold characteristics, DAC specifications, ADC specifications, Mixed signal layout issues: floorplanning, power supply and grounding issues, fully differential design/ matching, guard rings,shielding,interconnect considerations**.**

ModuleII :   **(10Hrs)**
DAC architectures: Resistor string, R-2R ladder networks, Current steering, Charge-scaling,Pipeline.ADCarchitectures:Flash,Pipeline,Dualslope,Successiveapproximation,OversamplingADC.

ModuleIII :   **(10Hrs)**
Data converter modeling: Sampling and aliasing: A modeling approach, Impulse sampling,AAF and RCF, Time domain description of reconstruction, The sample and hold, S/H spectralresponse, Circuit concerns for implementing S/H. Quantization noise, RMS quantization noisevoltage, treating quantization noise as a random variable, calculating RMS quantization noisevoltage from a spectrum

ModuleIV: **(10Hrs)**
Data converter SNR: Effective number of bits, Signal to noise plus distortion ratio, Spuriousfree dynamic range, dynamic range, SNR & SNDR, Clock jitter, Averaging to improve SNR,Spectral density view, Jitter and averaging, Relaxed requirements on AAF, Data converterlinearityrequirements,AddingnoisedithertoADCinput,DecimatingfiltersforADC.Decimating filters for ADCs, Interpolating filters for DACs. Noise-shaping data converters:Firstordernoiseshaping,Secondordernoiseshaping,Noiseshapingtopologies:Higher-order
modulators,Miltibitmodulators,Cascadedmodulators.

References:

1. BakerRJ,"CMOS:MixedSignalCircuitDesign",Secondedition,WileyIEEEPressPublications.

2. BakerRJ,"CMOS:CircuitDesign,LayoutandSimulation",Secondedition,WileyIEEEPressPublications.

3. Allen,PhillipE.,Holberg,DouglusR.,"CMOSAnalogCircuitDesign",OxfordUniversityPress Publications.

LaboratoryAssignments/Experiments:

1. Plotidealtransfercurvesfor3bitand4bitDAC,usingV_{Ref}=5Vand3V.FindtheresolutionforaDACif theoutput voltageis desiredto changein 1mV increments.
2. For3bitADC,V_{Ref}=5V,Plotideal transfer curveandquantization error.
3. Plottransfercurveandquantizationerrorbyshiftingentiretransfercurveofexample2,leftby1/2LSB and calculateDNL.
4. Designandsimulateanti-aliasingfilterwithtwoinputsinewaveshavingfrequencies4MHz and40 MHz.
5. Designandsimulate sampleand holdcircuit,with8MHz sinewavesampledat100 MHz.
6. CalculateSNRandplotADCinputandDACoutputforcascaded8bitADCandDACoperatedon VDD=1.5V,Vin =24mV(0.75VPP) andSamplingfrequency=100MHz.

504710-4 Embedded Signal Processor Architectures (Elective II)
Credits: 5

Teaching Scheme:

Lecture: 4Hrs/week

Examination Scheme:

In-Sem   : 50 Marks
End-Sem   : 50 Marks

Course Objectives:
1. To impart knowledge on the theoretical aspects of signal analysis and processing
2. To explore DSP Processor architectures
3. To understand DSP algorithms
4. To elaborate real world DSP applications

Course Outcomes:
On completion of the course, student will be able to-
1. Designing system with linear filters using DFT
2. Develop technical abilities of designing any application with FIR and IIR filters
3. Port algorithms on DSP Processor Platforms
4. Design Adaptive filters
5. Analyze filter structures

Course Contents

Module I :   (10 Hrs)
Signal Analysis and Processing: Discrete Fourier Transform, Fast Fourier Transform, Design of FIR Filters using windowing technique, Design of IIR Filters through Impulse invariance and bilinear transformation technique, Algorithms of Adaptive Filters, Design and Applications of Adaptive Filters.

Module II :   (10 Hrs)
Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, Real time implementation Considerations, Memory System and Data Transfer, Code Optimization.

Module III :   (10 Hrs)
Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph. Iteration bounds: Critical Path, Loop Bound, Algorithm to compute iteration bound, Longest Path Matrix (LPM).

Module IV: (10 Hrs)
Practical DSP Applications: Audio Coding and Audio Effects, Digital Image Processing, Two-Dimensional Filtering, Image Enhancement, DTMF generation and detection, FFT algorithms, Wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction.

References:

1. Woon-SengGan,SenM.Kuo,"EmbeddedSignalProcessingWiththeMicroSignalArchitecture",Wiley-IEEE Press.
2. KuoSenM,Woon-SengGan,"DigitalSignalProcessors:Architectures,Implementationsand Applications",Prentice-Hall.
3. ProakisJG,ManolakisDG,"DigitalSignalProcessing,Principles,AlgorithmsandApplications",Prentice-Hall.
4. LawrenceR.R,BernardGold,"TheoryandApplicationofDigitalsignalProcessing",Prentice-Hall.
5. ParhiKeshab,"VLSIDigitalSignalProcessingSystem",WileyPublication.

LaboratoryAssignments/Experiments:

1. Design andsimulate Npoint FFTbytargetingDSP processorplatform.
2. Designandsimulate NtapFIRfilterbytargetingsuitable DSP processorplatform.
3. Design andsimulateLMSadaptivefilter.
4. DesignasystemforDTMFsignaldetection.WriteaprogramtodetecttheDTMFsignalusingGoertzel algorithm
5. Performancecomparisonofdifferentfilterstructure.
6. Record a speech file in your own voice with sampling frequency of 8000 Hz. Design asystem to decompose a speech signal using Daubechies wavelet using wavelet packetdecomposition. Write a program to implement the system and plot the speech signalpassedvia each wavelet filter.

504710-5 **RealTimeOperatingSystems(ElectiveII)**
Credits:05

TeachingScheme: **ExaminationScheme:**

Lectures:4Hrs/week   **In-Sem   :50Marks**
                                                End-Sem   :50Marks

CourseObjectives:

1. TounderstandsoftwareArchitectureandDevelopment cycleofOperatingSystems
2. Tolearnvarious managementattributesof OperatingSystem
3. TounderstandRTOS
4. TostudyLinux/RTLinuxenvironment

CourseOutcomes:

Oncompletion ofthe course, studentwill beable to-

1. ListEmbeddedSoftwareDevelopmentsTools
2. LearnSoftwareDevelopmentProcess LifeCycle
3. GainknowledgeofReal TimeOperatingSystemswithrespecttouCOS
4. UnderstandRT LinuxoperatingSystem

CourseContents

ModuleI :   **(10 Hrs)**
SoftwareArchitectures,SoftwareDevelopmentsTools,ProgrammingConcepts,EmbeddedProgram
minginCandC++,Queues,Stacks,OptimizationofMemoryneeds,ProgramModelingConcepts,Soft
wareDevelopmentProcessLifeCycleanditsModel,SoftwareAnalysis,Designand Maintenance

ModuleII :   **(10Hrs)**
OperatingSystemConcepts,Processes,Deadlocks,MemoryManagement,
Input/Output,Files,Security, the Shell, Recycling of Concepts. Operating system structure
Monolithic Systems:LayeredSystems, VirtualMachines,Exo-kernels,Client-Server Model

ModuleIII :   **(10Hrs)**
Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure,
TaskManagement,TimeManagement,IntertaskCommunication&Synchronization,MemoryManag
ement,and PortingµCos-II.

ModuleIV: **(10Hrs)**
Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes
andFilters, File Protections, Shell Programming, System Programming, RT Linux Modules,
POSIXThreads,MutexManagement, SemaphoreManagement.

References:

1. LabrossyJ.J,Lawrence,"µC/OS-II,TherealtimeKernel",R&DPublication.
2. DrPrasadKVKK,"EmbeddedRealTimeSystems:Concepts,Design&Programming",Dr eamtech Publication.
3. SimonD.E,"AnEmbeddedSoftwarePrimer",Pearsoneducation.
4. TanenbaumAS,"ModernOperatingSystems",PrenticeHall.
5. RajKamal,"EmbeddedSystemsArchitecture,Programminganddesign",TataMc-Graw-Hill.

LaboratoryAssignments/Experiments:

1. MultitaskinginµCOS-IIRTOSusingminimum3tasksonARM7.(µCOS-IIbasedExperiments).
2. SemaphoreassignalingandsynchronizingonARM7.(µCOS- IIbasedExperiments).
3. Writeaprogramfor4*4Matrix KeypadInterface(basedonLinux OperatingSystem).
4. Developcharacterdevicedriverfor GPIO(based on Linux OperatingSystem).
5. WriteaprogramforExternalInterrupt(basedonLinux OperatingSystem).

504711

Lab PracticeII
Credits:4

TeachingScheme: **ExaminationScheme:**

Lectures:4Hrs/week   **TermWork**
                                                       :50MarksOr
                                                       al   :50Marks

The laboratory work will be based on completion of minimum two assignments/experimentsconfinedto thecourses of thesemester.

504712   **SeminarI**

Credits:4

TeachingScheme: **ExaminationScheme:**

Lectures:4Hrs/week   **TermWork**

                                               :50MarksO
ral   **:50Marks**

Seminar I: Shall be on state of the art topic of student's own choice approved by an authority.The student shall submit the duly certified seminar report in standard format, for satisfactorycompletionoftheworkdulysignedbytheconcernedguideandheadoftheDepartment/Institute.

604701   **TestingandVerificationofVLSICircuits**
Credits:4

TeachingScheme: **ExaminationScheme:**

Lectures:4Hrs/week   **In-Sem   :50Marks**
                                                          End-Sem   :50Marks

CourseObjectives:
1. Tointroducedesignprocessin VLSI
2. Tounderstandthelogical andFaultsimulationmodels
3. Tolearntechniques for design of testability
4. Tostudyhardwareand softwareverification issues fortesting

CourseOutcomes:
Oncompletion ofthe course,student willbe ableto-
1. Acceptchallenges inVLSITestingatdifferentabstractionlevels
2. Understandfaultmodelsfor generationoftestvectors
3. Calculateobservabilityand controllabilityparametersof circuit
4. Enhancetestabilityof acircuit
5. Usesimulation techniques fordesigningand testingofVLSIcircuits
6. Identifycharacteristicsof verificationmethods

CourseContents

ModuleI :   **(10Hrs)**
Introduction to the concepts and techniques of VLSI (Very Large Scale Integration) designverification and testing,VLSI testing process and test equipment, test economics and productquality,fault modeling,testingandverification in VLSIdesign process.
ModuleII :   **(10 Hrs)**
Test methods, logic and fault simulation, modeling circuits for simulation, algorithms for true-value simulation, algorithms for fault simulation, statistical methods for fault simulation,testability measures , combinational circuit test generation, sequential circuit test generation,memorytest.
ModuleIII :   **(10Hrs)**
Designfortestability,ScanandBoundaryscanarchitectures,Built-inSelf-test(BIST)andcurrent-basedtesting,analogtest bus standard.
ModuleIV: **(10Hrs)**
Systemtestandcore-baseddesign,ATPG,Embeddedcoretestfundamentals.Designverification techniques based on simulation, analytical and formal approaches. Functionalverification. Timing verification. Formal verification. Basics of equivalence checking andmodelchecking. Hardwareemulation.

References:

1   Bushnell M L, Agrawal V D, "Essentials of Electronic Testing for Digital, Memory andMixed-SignalVLSICircuits", KluwerAcademicPublishers.

2   AbramoviciM,BreuerMAandFriedmanAD,"DigitalsystemsandTestable Design",JaicoPublications.

3   CrouchAL,"DesignTestforDigitalIC'sandEmbeddedCoreSystems",PrenticeHall.
4   KropfT,"IntroductiontoFormalHardwareVerification,"SpringerPublications.

LaboratoryAssignments/Experiments:
1.   WriteVHDL/VerilogcodeforMUX-DscancellandLevelSensitive/edgetriggeredMUX-D scan cell.
2.   Write a VHDL/Verilog code torealize functioning of clocked scan cellandLSSDscancelldesign.
3.   Todevelopanexhaustivetestbenchforlowerlevelcombinationaldesigns:a.Adderand b.Multiplexer.
4.   ToprepareacompleteTestvectorsetforallpossiblestuckatfaultsparitycheckerwherethedata word is of 2-bit.

604702   **ASIC Design**

Credits:4

TeachingScheme: **ExaminationScheme:**

Lectures:4Hrs/week   In-Sem   :50Marks
                                                          End-Sem   :50Marks

CourseObjectives:

1. Togainknowledgeoftheprocess ofdesigningapplicationspecificalgorithm forASIC
2. TosynthesizedesignsinEDAtoolenvironment
3. Tolearndesignmethodologies,simulationand verification
4. Tolearnissuesin MixedsignalASICdesign

CourseOutcomes:
Oncompletion ofthe course, studentwill beable to-
   1. UnderstandconceptsandtechniquesofASICmodelingandsynthesis
   2. Perform statictiminganalysis,delayestimation andsynchronization
   3. LearnASICConstructionandtestingtechniques

CourseContents

ModuleI :   **(10 Hrs)**
ASIC Modeling and Synthesis :IC Design Technologies, Types of ASIC and Comparisons,ASIC Design Flow, Logic Synthesis, Simulation, EDA Tools, HDL Based logic Design andTestbench, library, logiclevel optimization.

ModuleII :   **(10Hrs)**
ASICPhysicalDesign:SystemSpecifications,ArchitectureDesign,LogicandCircuitDesign,
Physical   Design,   CAD   Tools,   System   partitioning,   Estimating   ASIC   Size,
PowerDissipation,PartitioningStrategies, Floorplanning,Placement,Routing,DesignReuse.

ModuleIII :(10Hrs)
ASICTimingAnalysis:Statictiminganalysis,Timingconstraints,falsepathdetection,Timingopti mization,ASIClibrarydesign,Delayestimation,mixedmodedesignandsimulation, SIissues.

ModuleIV: **(10Hrs)**
ASIC Verification and Testing:Different Chip Test Methods, Fault Models, Scan Test, PartialTest, Digital scan standards, BIST architecture, Memory Testing, BILBO, Boundary Scan,Self Test, JTAG, ATPG. Mixed Signal ASIC Design: Mixed Signal ASIC Design, Practicalaspects of mix analog digital design, Gate level mixed mode simulation. A brief introductiontosignal integrityeffectsin ASICdesign,Synthesis and Testing.

 References:
 1   SmithMichael,"ApplicationSpecificIntegratedCircuits"PearsonEducation.
 2   SoinRS,MalobertiF,FrancaJ,"Analogue-
     digitalASICs:circuittechniques,designtoolsandapplications", IEE Publications.
 3   SinghRaminderpal,"SignalIntegrityEffectsinCustomICandASICDesigns",WileyPublicati ons.

LaboratoryAssignments/Experiments:

1. WriteHDLcodeto simulate, synthesis,and place &routememoryon PLD.Checkresultsandalso write thetest bench.
2. WriteHDLcodetosimulate,synthesis,place &routeFIFOonPLD.Checkresultsandalsowrite thetest bench.
3. DrawCMOSlayout&simulateshiftregisterbyapplyingDRC'sofappropriatefoundryusingbackend tool and check the output.
4. Draw CMOS layout & simulate 16:1 MUX by applying DRC's of appropriate foundryusingbackend tool and check the output.
5. SimulateStuckatfault modelofgivenfunction.

Elective-III

Select one subjects from Group-I, and one subject from Group-II fromthefollowing list asElective-III.

Group		Subject	Credit
I	1	ValueEducation,HumanRightsandLegislativeProcedures	3
	2	EnvironmentalStudies	3
	3	RenewableEnergyStudies	3
	4	DisasterManagement	3
	5	KnowledgeManagement	3
	6	ForeignLanguage	3
	7	EconomicsforEngineers	3
	8	EngineeringRisk–BenefitAnalysis	3
II	1	OptimizationTechniques	2
	2	FuzzyMathematics	2
	3	DesignandAnalysisofAlgorithms	2
	4	CUDA	2

604703-1   ValueEducation,HumanrightsandLegislativeprocedures(ElectiveIII)
Credits:3

Teaching   **ExaminationScheme*:**
Scheme:Lectures:3Hr   **In-Sem   :50Marks**
s/Week   **End-Sem   :50Marks**

ModuleI :   (8Hrs)

Values and Self Development-Social values and individual attitudes, Work ethics,Indianvisionofhumanism,Moralandnonmoralvaluation,Standardsandprinciples,Valuej udgments.Importance of cultivation of values, Sense of duty, Devotion, Self-reliance,Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity, Power of faith,Nationalunity, Patriotism,Lovefornature, Discipline.

ModuleII :   (8Hrs)

Personality and Behavior Development-Soul and scientific attitude, God and scientificattitude,Positivethinking,Integrityanddiscipline,Punctuality,Loveandkindness,Avoi dingfaultfinding,Freefromanger,Dignityoflabor,Universalbrotherhoodandreligious tolerance, True friendship, Happiness vs. suffering love for truth, Aware of selfdestructivehabits, Association and cooperation, Doingbest, Savingnature.

ModuleIII :   (8 Hrs)

Human Rights-Jurisprudence of human rights nature and definition, Universal protection ofhuman rights, Regional protection of human rights, National level protection of humanrights, Human rights and vulnerable groups. Legislative Procedures-Indian constitution,Philosophy,fundamentalrightsandduties,Legislature,ExecutiveandJudiciary,Cons titution and function of parliament, Composition of council of states and house ofpeople,Speaker,Passingofbills,Vigilance,Lokpaland functionariesReferences

References

1. Chakraborty,S.K.,ValuesandEthicsforOrganizationsTheoryandPractice,OxfordUniversity Press,NewDelhi, 2001.

2. Kapoor,S.K.,HumanrightsunderInternationalLawandIndianLaw,PrenticeHallofIndia, NewDelhi, 2002.

3. Basu,D.D.,IndianConstitution,OxfordUniversityPress,New Delhi,2002.

4. Frankena,W.K.,Ethics,PrenticeHallof India, NewDelhi,1990.

5. MeronTheodor,HumanRightsandInternationalLawLegalPolicyIssues,Vol.1and2,Ox ford UniversityPress, New Delhi, 2000.

604703-2 **Environmentalstudies(ElectiveIII)**
Credits:3

Teaching Scheme:Lectures:3Hrs/Week

ExaminationScheme*:
In-Sem :50Marks
End-Sem :50Marks

ModuleI : **(8 Hrs)**

IntroductionandNaturalResources:Multidisciplinarynatureandpublicawareness,Renewablean dnonrenewalresourcesandassociatedproblems,Forestresources,Waterresources,Mineralresour ces,Foodresources,Energyresources,Landresources,Conservation of natural resources and human role. Ecosystems:Concept,Structure andfunction, Producers composers and decomposers, Energy flow, Ecological succession, Foodchains webs and ecological pyramids, Characteristics structures and functions of ecosystemssuchas Forest, Grassland, Desert, Aquaticecosystems.

ModuleII : **(8 Hrs)**

Environmental Pollution-Definition, Causes, effects and control of air pollution, waterpollution,soilpollution,marinepollution,noisepollution,thermalpollution,nuclearhazards, humanroleinpreventionofpollution,Solidwastemanagement,Disastermanagement,floods, earthquake, cycloneand landslides.

ModuleIII : **(8 Hrs)**

Socialissues and Environment-Unsustainable to sustainable development, Urban problemsrelated to energy, Water conservation and watershed management, Resettlement and re- habitation,Ethics,Climatechange,Globalwarming,Acidrain,Ozonelayerdepletion,Nuclear accidents, holocaust, Wasteland reclamation, Consumerism and waste products,Environment protection act, Wildlife protection act, Forest conservation act, Environmentalissues in legislation, population explosion and family welfare program, Environment andhumanhealth,HIV,Womenandchildwelfare,Roleofinformationtechnologyinenvironmentan d humanhealth.

References
1. Agarwal,K.C.,"EnvironmentalBiology",NidiPublicationLtd.,Bikaner,2001.
2. BharuchaErach,"BiodiversityofIndia,"MapinPublishingPvt.Ltd.,Ahmadabad,2002.
3. Bukhootsow,B.,"EnergyPolicyandPlanning",PrenticeHallofIndia,NewDelhi,2003.
4. Cunningham,W.P.,"EnvironmentalEncyclopedia",JaicoPublishingHouse,Mumbai, 2003.

604703-3   **RenewableEnergyStudies(ElectiveIII)**
                                    Credits:3

**Teaching
Scheme:Lectures:3H
rs/Week**

ModuleI:SolarEnergy: **(8 Hrs)**
PhotovoltaicSystems:IntroductiontotheMajorPhotovoltaicSystemTypes,Current–
VoltageCurvesforLoads,Grid-ConnectedSystems:InterfacingwiththeUtility,DCandAC   Rated
Power, The "Peak-Hours" Approach to Estimating PV Performance, CapacityFactors for PV
Grid Connected Systems¸ PV Powered Water Pumping, PV systems– offgridsystems and
scopeforinclusivegrowthof ruralIndia.

ModuleII:WindEnergy: **(8 Hrs)**
Wind Energy: wind speed and power relation, power extracted from wind, wind distributionand
wind speed predictions. Wind power systems: system components, Types of
Turbine,Choiceofgenerators,electricalloadmatching,powercontrol,Effectofwindspeedvariations,
tower height and its effect, Variable speed operation, maximum power operation,controlsystems,
Designconsideration ofwindfarms and control

ModuleIII:OtherEnergySources: **(8Hrs)**
Biomass – various resources, energy contents, technological advancements, conversion
ofbiomass in other form of energy – solid, liquid and gases. Gasifiers, Biomass fired boilers,Co-
firing, Generation from municipal solid waste, Issues in harnessing these sources. Miniand
micro hydel plants scheme layout economics. Tidal and wave energy, Geothermal andOcean-
thermal energy conversion (OTEC) systems – schemes, feasibility and viability. Fuelcell-types
andoperatingcharacteristics, efficiency, energyoutputof fuel cell

References

1. Renewable energytechnologies-R.Ramesh, NarosaPublication.
2. EnergyTechnology– S.Rao, Parulkar
3. Non-conventionalEnergySystems–Mittal,WheelersPublication.
4. ClarkW.Gellings,"TheSmartGrid:EnablingEnergyEfficiencyand
   DemandResponse",CRCPress
5. RenewableEnergyTechnologies–ChetanSingh Solanki,PHILearningPvt.Ltd.

604703-4   **DisasterManagement   (ElectiveIII)**
                              Credits:3

Teaching   **ExaminationScheme*:**
Scheme:Lectures:3Hr   **In-Sem   :50Marks**
s/Week   **End-Sem   :50Marks**

ModuleI :   **(8 Hrs)**
Introduction:Concepts and definitions: disaster, hazard, vulnerability, risk, capacity, impact,prevention, mitigation).Disasters classification; natural disasters (floods, draught, cyclones,volcanoes, earthquakes,tsunami, landslides, coastal erosion, soil erosion, forest fires etc.);manmade disasters (industrialpollution, artificial flooding in urban areas, nuclear radiation,chemical spills etc); hazard and vulnerability profile of India, mountain and coastal areas,ecologicalfragility

ModuleII :   **(8Hrs)**
Disaster Impacts :Disaster impacts (environmental, physical, social, ecological, economical,political, etc.); health,psycho-social issues; demographic aspects (gender, age, special needs);hazardlocations; globalandnational disastertrends; climate-changeand urbandisasters.

ModuleIII :   **(8 Hrs)**
Disaster Risk Reduction (DRR):Disaster management cycle–its phases; prevention,mitigation,preparedness,reliefandrecovery;structuralandnon-
structuralmeasures;riskanalysis,vulnerabilityandcapacityassessment;earlywarningsystems,Post-disasterenvironmental response (water, sanitation,food safety, waste management, disease control);Rolesandresponsibilitiesofgovernment,community,localinstitutions,NGOsandotherstak eholders; Policies and legislation for disasterrisk reduction, DRR programmes in India andtheactivities ofNationalDisaster Management Authority.

References
1. http://ndma.gov.in/(HomepageofNationalDisasterManagementAuthority).
2. http://www.ndmindia.nic.in/(NationalDisastermanagementinIndia,MinistryofHomeAffairs).
3. PradeepSahni,2004,DisasterRiskReductioninSouthAsia,PrenticeHall.
4. SinghB.K.,2008,HandbookofDisasterManagement:techniques&Guidelines,RajatPublicatio n.
5. GhoshG.K.,2006, DisasterManagement,APHPublishingCorporation.

604703-5   **KnowledgeManagement(ElectiveIII)**
                                    Credits:3

Teaching   **ExaminationScheme*:**
Scheme:Lectures:3H   **In-Sem   :50Marks**
rs/Week   **End-Sem   :50Marks**

ModuleI :   **(8 Hrs)**

Introduction:Definition,evolution,need,drivers,scope,approachesinOrganizations,strategiesin organizations, components and functions, understanding knowledge; Learningorganization:fivecomponentsoflearningorganization,knowledgesources,anddocumentatio n.EssentialsofKnowledgeManagement;knowledgecreationprocess,knowledgemanagementtechniq ues, systems and tools.

ModuleII :   **(8 Hrs)**

Organizational knowledge management; architecture and implementation strategies, buildingtheknowledgecorporationandimplementingknowledgemanagementinorganization.Knowl edge management system life cycle,managing knowledge workers, knowledge audit,andknowledgemanagement practicesin organizations, fewcasestudies

ModuleIII :   **(4 Hrs)**

FuturisticKM:KnowledgeEngineering,TheoryofComputation,DataStructure.

References

1.   KnowledgeManagement–aresourcebook –AThohothathriRaman,Excel,2004.
2.   KnowledgeManagement-EliasM.AwadHasanM.Ghazri,PearsonEducation
3.   TheKMToolkit–
      OrchestratingIT,Strategy&KnowledgePlatforms,AmritTiwana,Pearson,PHI,IIEdn.
4.   TheFifthDisciplineFieldBook   –
      Strategies&ToolsForBuildingAlearningoganizationPeterSenge etal. Nicholas
      Brealey1994
5.   KnowledgeManagement–SudhirWarier,Vikaspublications
6.   LeadingwithKnowledge,MadanmohanRao,TataMc-GrawHill.

604703-6   **ForeignLanguage   (ElectiveIII)**
                          Credits:3

Teaching Scheme:Lectures:3Hrs/Week	**ExaminationScheme*:** **In-Sem :50Marks** **End-Sem :50Marks**

ModuleI :   (8Hrs)

Pronunciationguidelines;Singlevowels,Accentuatedvowels,Vowelsandconsonantscombinations, Consonants;   Numbers   1-10   Articles   and   Genders;   Gender   in   French, Pluralarticles,Someusualexpressions.PronounsandVerbs;Theverbgroups,Thepronouns,Presenttense,SomecolorAdjectivesandPlural;Adjectives,Someadjectives,Ourfirstsentences,MoreNumbers.

ModuleII :   (8Hrs)

SentencesStructures;SomePrepositions,NormalSentences,NegativeSentences,InterrogativeSentences,ExercisesTheFamily;Vocabulary,Conversation,NotesonPronunciation, Notes on Vocabulary, Grammar, Liaisons Guideline. D'oùviens-tu (Where doyou come from); Vocabulary, Conversation,   Notes   on   Vocabulary,Liaisons   Guidelines.Comparer (Comparing);Vocabulary,Conversation,   Notes   on   Vocabulary,   Grammar LiaisonsGuidelines,Ordinal Numbers

ModuleIII :   (8 Hrs)

Le   temps   (Time);Vocabulary,Grammar,Time   on   the   clockAdditional   French Vocabulary;Vocabulary related to-The Family,Vocabulary related to-Where do you come from?French Expressions and Idioms;Day-to-day Life,At Work,The car,Sports, Specia EventsOther French Flavours;Nos cousins d'Amérique-Québec et Accadie, Au pays de labière etdesfrites, Mettez-vousàl'heureSuisse, Vé,peuchère, le françaisbiendechez nous

References

http://www.jump-gate.com/languages/french/index.html

604703-7   **EconomicsforEngineers   (ElectiveIII)**
                                      Credits:3

Teaching   **ExaminationScheme:**
Scheme:Lectures:3Hr   **In-Sem   :50Marks**
s/Week   **End-Sem   :50Marks**

ModuleI :(8 Hrs)
Introductiontothesubject:MicroandMacroEconomics,RelationshipbetweenScience,Engineering,
Technology and Economic Development. Production Possibility Curve, Nature ofEconomic
Law, Time Value of Money: concepts and application. Capital budgeting; Traditionaland
modern methods, Payback period method,IRR, ARR, NPV, PI (with the help of casestudies)

ModuleII :   **(8Hrs)**
Meaning of Production and factors of production, Law of variable proportions and returns
toscale.Internalandexternaleconomiesanddiseconomiesofscale.Conceptsofcostofproduction,
different types of costs; accounting cost, sunk cost, marginal cost, Opportunity cost.Break even
analysis,   Make   or   Buy   decision   (case   study).Relevance   of   Depreciation
towardsindustry.Meaning of market, types of market, perfect competition, Monopoly,
Monopolistic,Oligopoly. (Main features).Supply and law of supply, Role of demand and supply
in pricedetermination.

ModuleIII :   **(8 Hrs)**
Indian Economy, nature and characteristics. Basic concepts; fiscal and monetarypolicy,
LPG,Inflation, Sensex, GATT, WTO and IMF. Difference between Central bank and
Commercialbanks

References :
   1. JainT.R.,EconomicsforEngineers,VKPublication
   2. SinghSeema,EconomicsforEngineers,IKInternational
   3. ChopraP.N.,PrincipleofEconomics,KalyaniPublishers
   4. DewettK.K.,Moderneconomictheory,S.Chand
   5. H.L. Ahuja.,Moderneconomictheory,S.Chand

604703-8   Engineering risk–BenefitandAnalysis(ElectiveIII)
Credits:3

Teaching	ExaminationScheme*:
Scheme:Lectures:3Hrs/Week	In-Sem :50Marks End-Sem :50Marks

ModuleI :   (8 Hrs)

Introduction- Knowledge and Ignorance, Information Uncertainty in Engineering Systems,Introduction and overview of class; definition of Engineering risk;overview of Engineeringrisk analysis. Risk Methods: Risk Terminology, Risk Assessment, Risk Management andControl,RiskAcceptance,RiskCommunication,IdentifyingandstructuringtheEngineeringriskproblem;developingadeterministicorparametricmodelSystemDefinition and Structure: System Definition Models, Hierarchical Definitions of Systems,andSystem Complexity.

ModuleII :   (8Hrs)

Reliability Assessment:AnalyticalReliability Assessment,EmpiricalReliability AnalysisUsingLifeData, ReliabilityAnalysis of Systems

ModuleIII :   (8 Hrs)

Reliability and probabilistic risk assessment (RPRA), decision analysis (DA), and cost-benefitanalysis(CBA).Allofthesepertaintodecisionmakinginthepresenceofsignificant uncertainty. In ERBA, the issues of interest are: The risks associated with largeengineering projects such as nuclear power reactors, the International Space Station, andcriticalinfrastructures;thedevelopmentofnewproducts;thedesignofprocessesandoperationswith environmental externalities;and infrastructurerenewal projects.

References

1. Risk Analysis in Engineering and Economics, B. M. Ayyub, Chapman-Hall/CRCPress,2003.
2. Hoyland, Arnljot, and Rausand, Marvin. System Reliability Theory. Hoboken, NJ:WileyInterscience,1994.ISBN: 9780471471332.
3. Clemen,Robert,―MakingHardDecisions:AnIntroductiontoDecisionAnalysis(Business Statistics)― PHIpublications

604703-9   **OptimizationTechniques(ElectiveIII)**
Credits:2

Teaching Scheme:Lectures:2Hrs/Week

ModuleI :   **(6Hrs)**

First and second order conditions for local interior optima (concavity and uniqueness),Sufficient conditions for unique global optima; Constrained optimization with Lagrangemultipliers;Sufficient conditions foroptima withequalityand inequalityconstraints;

ModuleII :   **(8 Hrs)**

Recognizingandsolvingconvexoptimizationproblems.Convexsets,functions,andoptimization problems. Least-squares, linear, and quadratic optimization. Geometric andsemidefiniteprogramming.Vectoroptimization.Dualitytheory.Convexrelaxations.Approximation,fitting,andstatisticalestimation.Geometricproblems.Controlandtrajectoryplanning

Books:

1. StephenBoydandLievenVandenberghe,ConvexOptimization,CambridgeUniversityPress.
2. A. Ben-Tal, A. Nemirovski, Lectures on Modern Convex Optimization:Analysis,Algorithms,and EngineeringApplications, SIAM.
3. D.P.Bertsekas,A.Nedic,A.E.Ozdaglar,ConvexAnalysisandOptimization,AthenaScientific.
4. D.P.Bertsekas,NonlinearProgramming,AthenaScientific.
5. Y.Nesterov,IntroductoryLecturesonConvex Optimization:ABasicCourse,Springer.
6. J.BorweinandA.S.Lewis,ConvexAnalysisandNonlinearOptimization:TheoryandExamples, Springer.

604703-10   **FuzzyMathematics(ElectiveIII)**
                                 Credits:2

Teaching   **ExaminationScheme*:**
Scheme:Lectures:2Hr   **In-Sem   :50Marks**
s/Week   **End-Sem   :50Marks**

ModuleI :   **(8Hrs)**

Definition of a Fuzzy set; Elements of Fuzzy logic. Relations including,
Operations,reflexivity,symmetryandtransitivity;PatternClassificationbasedonfuzzyrelation
s

ModuleII :   **(6 Hrs)**

FuzzyModels:Mamdani,Sugeno,Tsukamoto

Books:

   1.Neuro-Fuzzyand SoftComputingbyS.R.Jung, Sun,Mizutani,

604703-11   DesignandAnalysis ofAlgorithm(ElectiveIII)
Credits:2

Teaching Scheme:Lectures:2Hrs/Week

ExaminationScheme*:
In-Sem   :50Marks
End-Sem   :50Marks

ModuleI :   **(8 Hrs)**

Introduction-Fundamentalcharacteristicsofanalgorithm.Basicalgorithmanalysis–Asymptotic analysis of complexity bounds– best, average and worst-case behaviour, standardnotations for expressing algorithmic complexity. Empirical measurements of performance,timeand spacetrade-offsin algorithms.

ModuleII :   **(8Hrs)**

Propertiesofbig-Ohnotation–Recurrenceequations–Solvingrecurrenceequations–Analysis   of linear search. Divide and Conquer: General Method – Binary Search – FindingMaximum and Minimum – Merge Sort – Greedy Algorithms: General Method – ContainerLoading–Knapsack

Books:

AlgorithmDesign–JonKleinbergandEvaTardosIntroductionto Algorithms–T.H.Corman

604703-B1	**CUDA**	**GroupII**
TeachingScheme:	**ELECTIVE-III**	**B**
Lectures2Hrs/Week		**ExaminationScheme:**
		Theory:50Marks(InSemester)
		50Marks(EndSemester)
		Credits:2

ModuleI :

History of GPUs leading to their use and design for HPC- The Age of Parallel Processing,The Rise of GPU Computing ,CUDA, Applications of CUDA, Development Environment,IntroductiontoCUDAC,Kernelcall,PassingParameters,QueryingDevices,UsingDeviceProperties

ModuleII:

ParallelProgramminginCUDAC-CUDAParallelProgramming,SplittingParallelBlocks,SharedMemoryandSynchronization,ConstantMemory,TextureMemory,CUDAevents, MeasuringPerformancewith Events.

Books:
1. Programming Massively Parallel Processors: A Hands-on Approach –second editionbyDavid
   B.Kirk,Wen-mei W.Hwu.
2. CUDAbyExample-AnIntroductiontoGeneral-PurposeGPUProgrammingbyJason Sanders ,EdwardKandrot-Addison Wesley
3. GPUComputingGemsEmeraldEdition-ApplicationsofGPUComputingSeriesbyWen-mei,
   W.Hwu
4. CUDAProgramming:ADeveloper'sGuidetoParallelComputingwithGPUsbyshanecook

604704   **Seminar II**
                                            Credits:4

TeachingScheme: **ExaminationScheme:**

4Hrs/Week   **TermWork :   50**
                                            MarksOral/Presentation:50
                                            Marks

Seminar II : shall be on the topic relevant to latest trends in the field of concerned branch,preferably on the topic of specialization based on the electives selected by him/her approvedby authority.The student shall submit the seminar report in standard format, duly certifiedforsatisfactorycompletionoftheworkbytheconcernedguideandheadofthe Department/Institute.

604705 Project Stage-I

Credits: 8

TeachingScheme: **ExaminationScheme:**

Lecture: 8Hrs/week   **TermWork**
                                                      :50Marks
                                              Oral :50 Marks

ProjectStage–I

Project Stage – I is an integral part of the project work. In this, the student shall complete thepartial work of the project which will consist of problem statement, literature review, projectoverview, scheme of implementation (Mathematical Model/SRS/UML/ERD/block diagram/PERT chart, etc.) and Layout & Design of the Set-up. As a part of the progress report ofProjectworkStage-
I,thecandidateshalldeliverapresentationontheadvancementinTechnologypertainingtothe selected dissertation topic.

The student shall submit the duly certified progress report of Project work Stage-I in standardformat for satisfactory completion of thework duly signed by the concerned guide and head oftheDepartment/Institute.

604706**Seminar III**

Credits:5

TeachingScheme: **ExaminationScheme:**

Lectures: 5Hrs/week   **Term   Work:50**
                                                                          MarksOral/   :   50
                                                                          MarksPresentation

SeminarIIIshallpreferablyanextensionof**seminarII.**Thestudentshallsubmittheduly   certified seminar report in standard format, for satisfactory completion of the work dulysignedbytheconcernedguide and headof theDepartment/Institute.

604707 **ProjectStage-II**
Credits:20

TeachingScheme: **ExaminationScheme:**

Lecture: 20Hrs/week **TermWork**
                                                      :150MarksO
                                              ral :50Marks

In Project Stage – II, the student shall complete the remaining part of the project which willconsistofthefabricationofsetuprequiredfortheproject,workstation,conductingexperimentsand takingresults, analysis&validation of results andconclusions.

The student shall prepare the duly certified final report of project work in standard format forsatisfactory completion of the work duly signed by the concerned guide and head of theDepartment/Institute.