Savitribai Phule Pune University, Pune

Maharashtra, India

Faculty of Science and Technology

Curriculum Structure and Syllabus

Master of Engineering (2025 Pattern) in

ME - Electronics & Communication (VLSI Design)

(With effect from Academic Year 2025-26)

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Abbreviations

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PO Programme Outcomes

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Master of Engineering in Electronics & Communication (VLSI Design) - 2025 Pattern

Preface by Board of Studies

Dear Students and Faculty Members,

We, the members of the Board of Studies of Electronics & Telecommunication engineering, are happy to present the syllabus for the Master of Engineering in Electronics and Communication Engineering (**VLSI Design)**, effective from the Academic **Year 2025–26** (2025 Pattern).

VLSI (Very Large-Scale Integration) is a pivotal and rapidly evolving domain that drives the development of modern electronic systems by integrating millions of transistors onto a single chip. It forms the foundation of advanced computing, high-speed communication, consumer electronics, artificial intelligence hardware, and embedded applications.

This curriculum has been carefully designed to provide students with a comprehensive understanding of digital and analog VLSI design, semiconductor device physics, design automation tools, verification techniques, and fabrication methodologies. It emphasizes both circuit-level and system-level design, fostering the skills required to build efficient, reliable, and scalable integrated circuits. By aligning with the latest technological advancements and industry demands, the program aims to prepare students for successful careers in areas such as ASIC/FPGA design, chip verification, semiconductor technology, embedded processors, and hardware accelerators.

The curriculum revision is mainly focused on knowledge component, skill-based activities, experiential learning and project-based activities. The revised syllabus falls in line with the objectives of Savitribai Phule Pune University, AICTE New Delhi, UGC, and various accreditation agencies by keeping an eye on the technological developments, innovations, and industry requirements. Learners are now getting sufficient time for self-learning either through online courses or additional projects for enhancing their knowledge and skill sets. We would like to place on record our gratefulness to the faculty, students, industry experts and stakeholders for having helped us in the formulation of this syllabus.

Dr. Suresh Shirbahadurkar
Chairman
Board of Studies - Electronics & Telecommunication Engineering

Members of Board of Studies, Electronics & Telecommunication Engineering, Savitribai Phule Pune University, Pune	
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Dr. Urmila Patil	Dr. D. Y. Patil Institute of Technology, Pimpri, Pune

Savitribai Phule Pune University
Curriculum Structure Semester I
M.E (Electronics and Communication-VLSI Design)

2025 Pattern

Course Code	Course Type	Course Name	Teaching Scheme		Examination Scheme					Credits		
			Theory	Practical	CCE	End Sem	Term	Oral	Total	Theory	Practical	Total
PCC-501- VLD	Program Core Course	Analog CMOS IC Design	4	-	50	50	-	-	100	4	-	4
PCC-502- VLD	Program Core Course	Digital CMOS IC Design	4	-	50	50	-	-	100	4	-	4
PCC-503- VLD	Program Core Course	MOS Device Modelling and Characterization	4	-	50	50	-	-	100	4	-	4
PCC-504- VLD	Program Core Course	VLSI Chip Design & Fabrication	4		50	50			100	4		4
PCC-505- VLD	Program Core Course – Lab	Design Lab -I	-	4	-	-	25	25	50	-	2	2
PEC-521- VLD	Program Elective Course	Elective I	3	-	50	50	-	-	100	3	-	3
PEC-522- VLD	Program Elective Course- Lab	Skill Based Lab-II		2			25	25	50		1	1
Total			**19**	**6**	**250**	**250**	**50**	**50**	**600**	**19**	**3**	**22**

List of Elective I Courses:

PEC-521A- VLD	Block Chain
PEC-521B- VLD	Nano Technology
PEC-521C- VLD	Wireless Sensor Networks
PEC-521D- VLD	Embedded Signal Processor Architecture

Savitribai Phule Pune University
Curriculum Structure Semester II
M.E (Electronics and Communication-VLSI Design)

2025 Pattern

Course Code	Course Type	Course Name	Teaching Scheme		Examination Scheme					Credits		
			Theory	Practical	CCE	End Sem	Term Work	Oral	Total	Theory	Oral	Total
PCC-551- VLD	Program Core Course	System on Chip	4	-	50	50	-	-	100	4	-	4
PCC-552- VLD	Program Core Course	Embedded Technology & IOT	4	-	50	50	-	-	100	4	-	4
PCC-553- VLD	Program Core Course	RFIC Design	4	-	50	50	-	-	100	4	-	4
PCC-554- VLD	Program Core Course – Lab	Design Lab–II	-	4	-	-	25	25	50		2	2
PEC-561- VLD	Program Elective Course	Elective –II	3	-	50	50	-		100	3	-	3
PEC-562- VLD	Program Elective Course	Elective –III	3	-	50	50	-		100	3	-	3
SEM- 571-VLD	Seminar	Technical Seminar 1	-	4	-	-	25	25	100		2	4
Total			**18**	**8**	**250**	**250**	**50**	**50**	**600**	**18**	**4**	**22**

List of Elective II Courses:

PEC-561A-VLD	Machine Learning	PEC-562A-VLD	Cloud Architecture Protocols
PEC-561B-VLD	Mixed Signal IC Design	PEC-562B-VLD	Fuzzy Mathematics
PEC-561C- VLD	Real Time Operating Systems	PEC-562C- VLD	Renewable Energy Studies
PEC-561D- VLD	Digital Image Processing and Pattern recognition	PEC-562D- VLD	Design and Analysis of Algorithms

List of Elective III Courses:

Savitribai Phule Pune University
Curriculum Structure Semester III
M.E (Electronics and Communication-VLSI Design)

2025 Pattern

Course Code	Course Type	Course Name	Teaching Scheme		Examination Scheme					Credits		
			Theory	Practical	CCE	End Sem	Term Work	Oral/ Presentation	Total	Theory	Practical	Total
RM-631-VLD	Research Methodology	Research Methodology	5		50	50			100	5		5
OJT-641- VLD	OJT /Internship	On Job Training /Internship		10			100		100		5	5
SEM-632- VLD	Seminar	Technical Seminar-II	-	6	-	-	25	25	50		3	3
RP-642- VLD	Research Project	Research Project-I	-	18	-	-	25	25	50	-	9	9
Total			**5**	**34**	**50**	**50**	**150**	**50**	**300**	**5**	**17**	**22**

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Curriculum Structure Semester IV
M.E (Electronics and Communication-VLSI Design)

2025 Pattern

Course Code	Course Type	Course Name	Teaching Scheme		Examination Scheme					Credits		
			Theory	Practical	CCE	End Sem	Term Work	Oral/ Presentation	Total	Theory	Oral	Total
SEM- 671-VLD	Seminar	Technical Seminar III	-	8	-	-	50	50	100	-	4	4
RP-681- VLD	Research Project	Research Project II	-	36	-	-	150	50	200	-	18	18
Total			**-**	**44**	**-**	**-**	**200**	**100**	**300**	**-**	**22**	**22**

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Semester I

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PCC-501-VLD: ANALOG CMOS IC DESIGN

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	CCEMarks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To provide a strong foundation in MOS device physics, modeling, and current mirror design for analog circuit applications
2. To introduce single-stage and differential amplifier configurations, emphasizing gain, frequency response, and common-mode issues.
3. To develop an understanding of CMOS op-amp architectures, compensation techniques, and low-power design considerations.
4. To familiarize students with analog signal processing blocks including bandgap references, switched-capacitor circuits, LNAs, and data converters.
5. To impart knowledge of analog layout techniques, parasitic effects, and EDA-based design flows for analog/mixed-signal ICs

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Analyze MOS device characteristics and design current mirror circuits considering noise and short-channel effects.
2. Design and evaluate amplifiers and differential pairs with appropriate gain and frequency response performance.
3. Design two-stage CMOS op-amps with stability, slew-rate, and output swing constraints.
4. Implement and analyze analog building blocks such as multipliers, mixers, and converters for SoC applications.
5. Apply layout principles and use CAD tools to perform post-layout simulations, parasitic extraction, and verification.

COURSE CONTENTS

UNIT-I	MOS Transistor Fundamentals	09Hrs

MOS Device Physics: Threshold voltage, Body effect, Short-channel effects, Large-signal and Small-signal Models, MOS Transistor as an Amplifier, Noise in MOS Devices (Thermal, Flicker, and Channel Noise),Current Mirrors: Basic, Cascode, Wilson, Wide-swing

UNIT-II	Basic Analog Building Blocks	09Hrs
Single-stage Amplifiers: Common Source, Common Gate, Source Follower, High-Gain Amplifier Architectures: Cascode and Folded-Cascode, Frequency Response of Amplifiers, Miller Effect, Differential Amplifiers: Single-ended and Differential Outputs, Common-Mode Rejection Ratio (CMRR) and Offset Issues		
UNIT-III	Operational Amplifier Design	09Hrs
Two-stage CMOS Op-Amp Design, Gain Boosting Techniques, Frequency Compensation: Miller Compensation, Pole-zero Cancellation, Slew Rate and Output Swing Considerations, Low-Power and Low-Voltage Op-Amp Design Approaches		
UNIT-IV	Analog Multipliers and Mixers	09Hrs
Bandgap Reference Circuits, Analog Multipliers and Mixers (Basic CMOS Implementations), Switched-Capacitor Circuits (Sample-and-Hold, Integrators), Low-Noise Amplifier (LNA) Basics in CMOS, Introduction to Data Converters: Flash ADC, Pipeline ADC, Current-Steering DAC, Case Study: Analog Building Blocks in Modern SoCs		
UNIT-V	Analog Layout and CAD Tools	09Hrs
Principles of Analog Layout: Matching, Symmetry, Common-centroid Layout, Parasitics in Analog Circuits: Capacitance, Resistance, Crosstalk, Layout Techniques for Current Mirrors, Differential Pairs, and Op-Amps Guard Rings, Shielding, and Latch-up Prevention, Noise Coupling and Substrate Effects in Mixed-Signal ICs, Design Flow Using EDA Tools (Cadence Virtuoso, Synopsys Custom Designer, Mentor Graphics), Post-layout Simulation, Parasitic Extraction, and Verification, Case Study: Layout-to-silicon issues in Analog CMOS ICs		
LEARNING RESOURCES		
1. P.K.Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002 2. M.L.Bushnell & V.D.Agarwal, “Essentials of Electronic Testing for Digital, Memory and Mixed signal VLSI Circuits”,Kluwer Academic Publishers, 2004 3. N.K Jha and S.G Gupta ,”Testing of Digital Systems”, Cambridge University Press, 2003. 4. Zainalabe Navabi, “Digital System Test and Testable Design: Using HDL Model and Architecture”, Springer,2010 5. Laung-Terng Wang,Cheng-Wen Wu,Xiaoqing Wen,VLSI ‘Test Principles and Architectures”, Morgan Kaufmann Publishers, 2006		

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PCC-502-VLD: DIGITAL CMOS IC DESIGN

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. Understand the advanced principles of CMOS logic design.
2. Develop an understanding of interconnect modeling in VLSI circuits
3. Explore modern design techniques for low power and high-performance circuits.
4. Develop methodologies for reliability-aware and robust VLSI circuit design
5. Impart knowledge of emerging VLSI design paradigms

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Analyze and optimize CMOS circuits for delay, power, and area.
2. Design complex digital subsystems using CMOS logic.
3. Apply low power techniques in digital design.
4. Identify and evaluate major reliability issues in nanoscale CMOS design such as HCI, BTI, SEU, and process variations
5. Develop testable and robust CMOS designs for industrial application.

COURSE CONTENTS

UNIT-I	CMOS Fundamentals	09Hrs

CMOS inverter: DC characteristics, switching threshold, Noise margins, propagation delay, power dissipation, Static and dynamic CMOS logic, Pseudo-NMOS, tri-state logic. Combinational and Sequential Logic Design: Design styles: static, dynamic, pass-transistor logic, Delay estimation and logical effort, Design of arithmetic circuits: adders (Ripple, CLA, Brent-Kung), multipliers (array, Wallace tree), Static and dynamic latches and flip-flops, Setup and hold times, clocking strategies, Pipelining and retiming, Metastability and synchronization

UNIT-II	Interconnect and Scaling Issues	09Hrs

Interconnect modeling: resistance, capacitance, delay, RC delay models, Elmore delay, Buffer insertion, wire sizing, repeater optimization, Scaling challenges in advanced nodes (FinFET, GAAFET)

UNIT-III	Low Power Design Techniques	09Hrs

Sources of power consumption, Clock gating, power gating, voltage scaling, Sub-threshold logic and multiple threshold voltages, Dynamic voltage and frequency scaling (DVFS), Physical Design and Layout, Layout design rules, stick diagrams, Transistor sizing and matching, Parasitic extraction, Floor planning, placement and routing issues.		
UNIT-IV	Advanced CMOS Technologies and Reliability	09Hrs
FinFET, GAAFET, SOI CMOS design, Reliability issues: hot carrier injection, bias temperature instability, soft errors, Process variations and design robustness, Aging effects and reliability-aware design.		
UNIT-V	Emerging Trends in Digital CMOS Design	09Hrs
3D ICs, Heterogeneous integration, Approximate computing and neuromorphic design, Energy harvesting and ultra-low power design, Hardware security in CMOS design (side-channel attacks, PUFs).		
LEARNING RESOURCES :		
1. Digital Integrated Circuits – Jan M. Rabaey, Anantha Chandrakasan 2. CMOS VLSI Design: A Circuits and Systems Perspective– Weste & Harris 3. Low Power CMOS Digital Design– Anantha Chandrakasan 4. Principles of CMOS VLSI Design– Neil Weste & Kamran Eshraghian 5. IEE Transactions and conference papers for current trends		

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PCC-503-VLD: MOS DEVICE MODELING AND CHARACTERIZATION

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To introduce the electrostatic principles and operational modes of MOS structures.
2. To study scaling challenges and short-channel effects in MOSFETs.
3. To understand transistor modeling using SPICE equations.
4. To explore capacitance-based MOSFET models and their comparisons.
5. To study advanced MOSFET modeling techniques and structures.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Explain MOS transistor operation, flat-band voltage, inversion, and small-signal capacitance.
2. Analyze short-channel effects and evaluate their impact on MOSFET performance.
3. Apply Level 1, 2, and 3 SPICE models for MOSFET simulation.
4. Differentiate various MOSFET models based on capacitance behavior.
5. Evaluate compact and advanced MOSFET models including FinFETs.

COURSE CONTENTS

UNIT-I	Electrostatic Principles and Operational Modes of MOS Structures	09Hrs

A qualitative Description of MOS Transistor operation, contact potentials, two terminal MOS structure: Flat band voltage, Potential balance and charge balance, Effect of Gate-Substrate voltage on Surface Condition, Inversion, Small signal capacitance

UNIT-II	MOSFET Scaling Challenges	09Hrs

Short channel MOSFET, Small Dimension Effects, Channel length Modulation, Barrier lowing two dimensional charge sharing and threshold voltage, Punch through, Carrier velocity Saturation, Hot carrier Effects, Scaling, Effects due to thin oxides and high doping, mobility degradation

UNIT-III	SPICE-Based Transistor Modeling	09Hrs

Modeling of Transistor using SPICE: Basic concepts, The level 1 Equations, The Level 2 Equations, The Level 3 Equations, Comparison of SPICE Models

UNIT-IV	MOSFET Models	09Hrs

Capacitance Models, Basic MOSFET models, Comparison of MOSFET Models		
UNIT-V	Advanced MOSFET Modeling Techniques	09Hrs
Advanced MOSFET models for circuit simulators, Surface potential models, inversion charge based models, Compact MOSFET models, threshold voltage-based model models, advanced MOSFET structures such as FINFET		
LEARNING RESOURCES:		
1. Yannis Tsividis, "Operation and modeling of the MOS transistor", Oxford University Press. 2. Kang S. M , "CMOS Digital Integrated Circuits", Tata Mc-Graw Hill. 3. Carlos Galup & Montoro, "MOSFET Modeling for Circuit Analysis and Design", World Scientific. 4. Donald Neamen, "Semiconductors Physics and Devices", Tata Mc-Graw Hill. 5. Sze S. M, "Physics of Semiconductor Devices, Second Edition, Wiley Publications		

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PCC-504-VLD: VLSI CHIP DESIGN & FABRICATION

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To understand Verilog and its use to the design various applications.
2. To analyze HDL design flow and EDA tools.
3. To analyze different aspects of testing and fault models.
4. To understand the insights of chip design such as epitaxy and lithography.
5. To understand the insights of chip design such as ion implantation and metallization

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Analyze and implement basic Verilog coding.
2. Understand the IC design flow and EDA tools
3. Understand the AISC timing analysis and different fault models.
4. Understand the major steps in the fabrication process of VLSI circuits
5. Apply implantation process for VLSI devices and discuss the metallization.

Prerequisite Courses : Digital Electronics, VLSI Design

COURSE CONTENTS

UNIT-I	Design with HDL	09Hrs

Basics of Verilog: Typical HDL-flow, why Verilog HDL, trends in HDLs. Gate-Level Modelling: Modelling using basic Verilog gate primitives, description of and/or and buffer/not type gates, rise, fall and turn-off delays, min, max, and typical delays. Behavioral Modelling: Structured procedures, initial and always, blocking and non- blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.

UNIT-II	ASIC Design Part I	09Hrs

Types of ASIC and Comparisons, ASIC Design Flow, Logic Synthesis, Simulation, EDA Tools, ASIC Physical Design : Architecture Design, Physical Design, CAD Tools, System partitioning, Partitioning Strategies, Floor planning, Placement, Routing

UNIT-III	ASIC Design Part II	09Hrs

ASIC Timing Analysis: Static timing analysis, Timing constraints, Delay estimation, ASIC Verification and Testing: Different Chip Test Methods, Fault Models, Scan Test, Partial Test, Digital scan standards, BIST architecture, BILBO, Boundary Scan, Self-Test, JTAG, ATPG

UNIT-IV	Chip Design	09Hrs

Crystal Growth and Wafer Preparation: Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing.

Epitaxy: Introduction, Vapour-Phase Epitaxy.

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography.

Reactive Plasma, Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Reactive Plasma-Etching Techniques and Equipment

UNIT-V	Chip Fabrication	09Hrs

Ion Implantation: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation.

Metallization: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization problems.

LEARNING RESOURCES :

Text Books:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.
2. S.M. Sze, VLSI Technology, McGraw-Hill, 2017, 2nd Edition (Indian).

ReferenceBooks:

1. Smith Michael, “Application Specific Integrated Circuits” Pearson Education
2. S.K. Gandhi, “VLSI Fabrication Principles”, John Willey &Sons

Laboratory Experiments

1. Write Verilog code and testbench to simulate, synthesis for the 4-bit counter [Synchronous & Asynchronous counter].
2. Write Verilog code and testbench to simulate, synthesis for 4/8-bit Magnitude Comparator
3. Write Verilog code and testbench to simulate, synthesis for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16.
4. Write Verilog code and testbench to simulate, synthesis Mealy and Moore Sequence Detector to detect Sequence. ------11101-----.
5. Verify the functionality of the code Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND, OR gates. Write test bench with appropriate input patterns to verify the modelled behaviour

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PEC-521A-VLD: Elective I : BLOCKCHAIN

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. Understand the fundamental concepts, architecture and cryptographic principles underlying blockchain and distributed ledger technologies.
2. Explore various consensus mechanisms to achieve secure and reliable agreement in decentralized systems.
3. Design and develop smart contracts, decentralized applications (DApps) .
4. Evaluate the application of blockchain frameworks in enterprise environments, decentralized finance (DeFi)
5. Explore advanced trends and research directions for integrating blockchain with IoT, AI and Cloud technologies.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. **A**nalyze the evolution, architecture, and cryptographic foundations of blockchain systems.
2. Design and evaluate smart contracts and decentralized applications (DApps),
3. Apply enterprise blockchain frameworks to evaluate cross-chain interoperability solutions.
4. Assess decentralized finance (DeFi) applications and challenges in blockchain adoption.
5. Investigate emerging blockchain research trends , integration with IoT, AI, and Cloud technologies.

Prerequisite Courses : Computer Networks, Data Structures and Algorithms, Distributed Systems

COURSE CONTENTS

UNIT-I	Blockchain Foundations & Cryptography	07Hrs

Evolution of blockchain: Bitcoin to Web3, Blockchain architecture: Blocks, chains, nodes, P2P network, Permissioned vs. permissionless blockchains, Distributed Ledger Technologies (DLT), Cryptographic principles:Hashing, Merkle Trees, Digital Signatures, Zero-Knowledge Proofs (zkSNARKs, zkSTARKs), Consensus mechanisms:Proof of Work (PoW), Proof of Stake (PoS), Delegated Proof of Stake (DPoS), Practical Byzantine Fault Tolerance (PBFT), Directed Acyclic Graphs (DAG)

UNIT-II	Smart Contracts & Decentralized Applications (DApps)	07Hrs
Smart contract fundamentals and design principles, Economic and legal aspects of smart contracts, Oracles and hybrid contracts: Conceptual overview, Security considerations: Common vulnerabilities, Mitigation strategies, Gas costs and optimization concepts		
UNIT-III	Enterprise Blockchain Frameworks & Cross-Chain Interoperability	07Hrs
Hyperledger Fabric, Corda, Quorum — architecture and use-cases, Cross-chain interoperability: Polkadot, Cosmos — concepts and industry relevance, Case studies and real-world examples.		
UNIT-IV	Decentralized Finance (DeFi), NFTs & Regulations	07Hrs
DeFi ecosystem, NFTs, DAOs, CBDCs — trends and conceptual frameworks, Regulatory frameworks: GDPR, KYC and AML, compliance challenges, Sustainability and green blockchain initiatives.		
UNIT-V	Advanced Trends-IoT, AI, Cloud Integration	07Hrs
Blockchain for IoT: Secure device identity, data integrity, Blockchain for AI: Data provenance, AI model trustworthiness, Blockchain for Cloud: case study of Decentralized storage, edge computing integration, Privacy-enhancing techniques: Mixers, ring signatures, confidential transactions.		

LEARNING RESOURCES :

Text Book:

1. Imran Bashir, *Mastering Blockchain*, 4th Edition, Packt Publishing, 2023.
2. Daniel Drescher, *Blockchain Basics: A Non-Technical Introduction in 25 Steps*, 1st Edition, Apress, 2017.
3. Andreas M. Antonopoulos, Gavin Wood, *Mastering Ethereum: Building Smart Contracts and DApps*, 1st Edition, O'Reilly Media, 2018.
4. Ritesh Modi, *Solidity Programming Essentials*, 2nd Edition, Packt Publishing, 2022.
5. Nitin Gaur, Luc Desrosiers, Venkatraman Ramakrishna, Petr Novotny, Anthony O'Dowd, *Hands-On Blockchain with Hyperledger: Building Decentralized Applications with Hyperledger Fabric and Composer*, 1st Edition, Packt Publishing, *2018.*
6. Nakul Shah, *Blockchain for Business with Hyperledger Fabric*, 1st Edition, Packt Publishing, 2018.

7. Arshdeep Bahga, Vijay Madisetti, *Blockchain Applications: A Hands-On Approach, 1st Edition, VPT, 2017.*

Reference Book :

1. Roberto Infante, Building Ethereum DApps, 1st Edition, Packt Publishing, 2019.
2. Kevin Solorio, Randall Kanna, David H. Hoover, Hands-On Smart Contract Development with Solidity and Ethereum: From Fundamentals to Deployment, 1st Edition, O'Reilly Media, 2019.
3. Debajani Mohanty, Corda in Action, 1st Edition, Manning Publications, 2021

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PEC-521B-VLD: Elective I - NANO TECHNOLOGY

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To introduce the fundamental science and principles underlying nanotechnology and nanoscale phenomena.
2. To study biological, chemical, physical and engineering aspects for designing nanoscale systems and devices.
3. To develop understanding of fabrication techniques, synthesis processes and characterization methods in nanotechnology.
4. To explore applications of nanostructures, sensors, MEMS/NEMS devices, and nano-enabled smart materials.
5. To prepare students for research and industrial applications in electronics, healthcare, energy, and materials engineering using nanotechnology.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Explain the fundamental science of nanotechnology, including biosystems, quantum effects, smart materials, and nanostructures.
2. Analyze nanosensors, nanostructures, and nanomaterial synthesis methods with their applications.
3. Describe carbon nanotubes, nanowires, and fabrication techniques for MEMS/NEMS devices.
4. Evaluate the working principles and applications of nanostructure devices such as tunneling diodes, FETs, and single-electron devices.
5. Apply advanced microscopy techniques like SPM and AFM for nanoscale characterization.

COURSE CONTENTS

UNIT-I	Fundamentals of Nanotechnology	07Hrs

The fundamental science behind nanotechnology, bio systems, molecular recognition, quantum mechanics & quantum ideas, optics. Smart materials & Sensors, self-healing structures, heterogeneous nano-structures & composites, encapsulations.

UNIT-II	Nano-Sensors and Structures	07Hrs
Natural nano-scale sensors, electromagnetic sensors, biosensors, electronic noses , Nanostructures, Micro/Nano-devices, nano-materials Synthesis and Applications		
UNIT-III	Introduction to Micro/Nanofabrication	07Hrs
Introduction to Carbon nano-tubes.- Nano-wires, Concept of Micro/Nanofabrication.- Stamping Techniques. Methods and Applications, Materials Aspects of Micro- and Nanoelectromechanical Systems,- MEMS/NEMS , Devices and Applications.		
UNIT-IV	Nanostructure devices	07Hrs
Nanostructure devices –Resonant tunneling diodes, Field-effect transistors, Single-electrode transfer device.		
UNIT-V	Microscopy and Types	07Hrs
Scanning Probe Microscopy, Noncontact Atomic Force Microscopy, Low Temperature Scanning Probe Microscopy.		
LEARNING RESOURCES :		
1. Springer Handbook of Nanotechnology 2. Rattner Mark , Rattner Daniel, “Nanotechnology: A Gentle Introduction to the Next Big Idea” 3. Kulkarni Sulbha K, “ Nanotechnology :Principals & Practices”, Capital Publications 4. Vlaimir Mitin, “ Introduction to nanoelectronics science, Nanotechnology, Engineering and Applications”, Cambridge University Press		

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PEC-521C-VLD: ELECTIVE-I-WIRELESS SENSOR NETWORKS

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To provide fundamental knowledge of wireless sensor networks, their motivation, and applications in real-world domains.
2. To study sensor node architecture, subsystems, and power management techniques.
3. To understand synchronization, security challenges, and solutions in WSNs.
4. To explore WSN operating systems, middleware, and prototype implementations.
5. To analyze physical layer, medium access control (MAC), and communication aspects in WSNs.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Explain the motivation, challenges, and applications of Wireless Sensor Networks in real-world domains.
2. Describe the architecture of a sensor node and apply power management techniques for efficient operation.
3. Analyze the need for time synchronization and evaluate security mechanisms in WSNs.
4. Compare different operating systems and middleware used in wireless sensor networks.
5. Analyze physical and MAC layer protocols for reliable communication in WSNs.

COURSE CONTENTS

UNIT-I	INTRODUCTION WSN	07Hrs

Motivation for a Network of Wireless Sensor Nodes, Sensing and Sensors Wireless Networks, Challenges and Constraints. Applications to: Health care, Agriculture, Traffic and others

UNIT-II	WSN ARCHITECTURE	07Hrs

Node Architecture; the sensing subsystem, processor subsystem, communication interface, LMote, XYZ Power Management - Through local power, processor, communication subsystems and other means		
UNIT-III	NETWORK SECURITY	07Hrs
Time Synchronization needs, challenges and solutions overview for ranging techniques. Security Fundamentals, challenges and attacks of Network Security, protocol mechanisms for security		
UNIT-IV	OPERATING SYSTEMS	07Hrs
Functional and nonfunctional Aspects, short overview of prototypes–Tiny OS, SOS, Contiki, LiteOS, Sensor grid		
UNIT-V	PROTOCOLS	07Hrs
Physical Layer- Basic Components, Source Encoding, Channel Encoding, Modulation, Signal Propagation. Medium Access Control –types, protocols, standards and characteristics, challenges.		
LEARNING RESOURCES:		
1. Dargie W., Poellabauer C., "Fundamentals of wireless sensor networks: theory and practice", John Wiley and Sons. 2. Sohraby K., Minol, D., Znati T., "Wireless sensor networks: technology, protocols, and applications", John Wiley and Sons. 3. Hart J. K. Martinez K., "Environmental Sensor Networks: A revolution in the earth system science", Earth-Science Reviews. 4. Feng Zhao, Leonidas J.Guibas, "Wireless Sensor Networks: An Information Processing Approach".		

Savitribai Phule Pune University
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PEC-521D-VLD: ELECTIVE-II- Embedded Signal Processor Architectures

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

- To study signal analysis and digital filter design techniques using DFT, FFT, FIR, IIR, and adaptive filters.
- To understand the fundamental building blocks of digital signal processing systems.
- To learn DSP processor architectures and their hardware/software integration.
- To represent DSP algorithms using various graph-based models and analyze computational bounds.
- To explore practical applications of DSP in audio, image, and communication systems.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Design and implement FIR, IIR, and adaptive filters for real-time signal processing applications.
2. Analyze and apply MAC units, ALU, multipliers, dividers, and shifters in DSP operations.
3. Select suitable DSP processors and interface them for application-specific designs.
4. Model DSP algorithms with block diagrams and graphs and compute iteration bounds for optimization.
5. Apply DSP techniques such as filtering, FFT, and wavelets in solving real-world signal and image processing problems.

COURSE CONTENTS

UNIT-I	Fourier Transforms and Adaptive Filtering in DSP	07 Hrs

Signal Analysis and Processing: Discrete Fourier Transform, Fast Fourier Transform, Design of FIR Filters using windowing technique, Design of IIR Filters through Impulse invariance and bilinear transformation technique, Algorithms of Adaptive Filters, Design and Applications of Adaptive Filters

UNIT-II	Introduction to Digital signal processing systems	07 Hrs
Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers		
UNIT-III	DSP Processor Architecture	07 Hrs
DSP processor architecture, Software developments, Selections of DSP processors, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX		
UNIT-IV	DSP Algorithm Representation	07 Hrs
Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph. Iteration bounds: Critical Path, Loop Bound, Algorithm to compute iteration bound		
UNIT-V	Advanced DSP Applications	07 Hrs
Practical DSP Applications: Audio Coding and Audio Effects, Digital Image Processing, Two-Dimensional Filtering, Image Enhancement, DTMF generation and detection, FFT algorithms, Wavelet algorithms		
LEARNING RESOURCES:		
1. Woon-Seng Gan, Sen M. Kuo, "Embedded Signal Processing With the Micro Signal Architecture", Wiley-IEEE Press. 2. Kuo Sen M, Woon-SengGan," Digital Signal Processors: Architectures, Implementations and applications", Prentice-Hall. 3. Proakis J G, Manolakis D G, "Digital Signal Processing, Principles, Algorithms and Applications", Prentice-Hall. 4. Lawrence R. R, Bernard Gold, "Theory and Application of Digital Signal Processing", Prentice-Hall. 5. Parhi Keshab , "VLSI Digital Signal Processing System", Wiley Publication		

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PCC-505-VLD: Design Lab-I

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	02	TW Marks: 25 Marks OR Marks : 25 Marks

COURSE OBJECTIVE:

1: To design basic building blocks for analog CMOS circuits.

2: To synthesize the building blocks of digital circuits and perform timing analysis targeting standard cell based semicustom design methodology.

3: To study FPGA based design methodology

4: To design I/O cells and interconnects.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. To extract device parameters (λ, gm) from I–V plots and analyze their impact on amplifier performance.
2. To evaluate speed, power, and area trade-offs in different logic gate design styles.
3. To develop hierarchical HDL design skills and validate modular design approaches.
4. To gain hands-on proficiency in industry-standard VLSI design and verification environments.
5. To demonstrate the ability to map HDL designs onto FPGA hardware and interface with external devices
6. To understand FPGA internal architecture and configure logic, I/O, and routing resources for custom designs

LABORATORY EXPERIMENTS (*Any 6)

Guidelines : From 1-6 :any 4 and From 7-10:any 2

1. To calculate lambda for PMOS & NMOS, Trans conductance plots, Single transistor amplifier with different loads.
2. To design and simulate logic gates using various logic styles and compare the performance.
3. To Design the following building blocks employing various architectures and develop HDL models: 32-bit Parallel adder using 8-bit adder module, 32-bit Shift register using 8-bit Shift register module.
4. To study EDA Tools: Cadence Tools, Synopsys Tools
5. To study and implement FPGA real time programming and I/O interfacing

6.	To study and implement CLB, IOB, Programmable Interconnect of Xilinx Devices.
7.	Write Verilog code and testbench to simulate, synthesis for the 4-bit counter [Synchronous & Asynchronous counter].
8.	Write Verilog code and testbench to simulate, synthesis for 4/8-bit Magnitude Comparator
9.	Write Verilog code and testbench to simulate, synthesis for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16.
10.	Write Verilog code and testbench to simulate, synthesis Mealy and Moore Sequence Detector to detect Sequence. ------11101-----.

LEARNING RESOURCES:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2nd Edition.
2. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2nd Edition.
3. Samir Palnitkar, Verilog HDL, Pearson Education, 2003, 2nd Edition
4. Joseph Cavanagh, Verilog HDL Design Examples, CRC Press, 2018
5. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, Kluwer Academic, 2002, 2nd Edition

Savitribai Phule Pune University Master of Engineering (2025 Course) – Electronics and Communication (VLSI Design)		
PEC-522-VLD: SKILL BASED LAB-I		
Teaching Scheme	Credits	Examination Scheme
Theory : 02 Hours/Week	01	TW Marks: 25 Marks OR Marks : 25 Marks
PREREQUISITE COURSES : Program Elective Course		
GUIDELINES FOR SKILL BASED LAB: Skill Based Laboratory are based on the electives chosen by the students		

LABORATORY EXPERIMENTS (*Any 3) FROM PART-A

Part A –Blockchain

1. Write a program to simulate a blockchain with multiple blocks using hashing and a simple Proof-of-Work mechanism.
2. Design and deploy a simple smart contract using Solidity on Remix IDE and test it on an Ethereum test network.
3. Simulate a consensus mechanism using Python or an online tool and demonstrate how nodes agree on the next block even in the presence of faulty nodes.

Part A –Nano Technology

1. Introduction of analysis and characterization of Nano structured materials, coating and thin film sensors.
2. Surface tension measurement of Nano fluids.
3. To observe the size and slope of the Nano sized sample using scanning electron microscopy.
4. Design, simulation and analysis of Nano structures.

Part A –Wireless Sensor Networks

1. Reading data from Sensor nodes.
2. Implement 50 stationary nodes topology using NS2 for data transmission and record QoS parameters of the Networks/ Test bed.
3. Implement 50 dynamic nodes topology using NS2 for data transmission and record QoS parameters of the Networks /Test bed.
4. On any above topology change the Network layer/Transport layer/MAC layer protocol and monitor the changes between any two protocols/ test bed using Network Simulator.

Part A –Embedded Signal Processor Architectures

1. Design and simulate N point FFT by targeting the DSP processor platform.
2. Design and simulate N tap FIR filter by targeting suitable DSP processor platform.
3. Design and simulate LMS adaptive filter.
4. Record a speech file in your own voice with a sampling frequency of 8000 Hz. Design a

system to decompose speech signals using Daubechies wavelet using wavelet packet decomposition. Write a program to implement **the** system and plot the speech signal passed via each wavelet filter.

MINPROJECT FROM PART-B

Part B-Blockchain –

1. To design and implement a blockchain-based voting system where votes are securely stored, tamper-proof, and transparently counted using Ethereum smart contracts

Part B - Nano Technology

1. Simulation of Nano-Biosensor for Disease Detection
2. Design and Analysis of Carbon Nanotube (CNT)-based Field Effect Transistor (CNT-FET)

Part B - Wireless Sensor Networks

1. Smart Agriculture Monitoring using Wireless Sensor Network
2. Secure & Time-Synchronized Wireless Sensor Network for Healthcare Monitoring

Part B -Embedded Signal Processor Architectures

1. Adaptive Noise Cancellation using LMS Algorithm
2. Simulation and Analysis of DSP-Based Audio Effects

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Maharashtra, India

ME (2025 Course) – Electronics & Communication (VLSI Design)

Semester II

Savitribai Phule Pune University
Master of Engineering (2025 Course) – Electronics and Communication
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PCC-551-VLD: SYSTEM ON CHIP

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To understand the basic concepts and models in SoC.
2. To explore Micro-programmed Architectures and SoC modeling.
3. To explore features of simulation and synthesis of RTL intent.
4. To learn recent trends in SoC design.
5. To enable students to understand the principles of IP-based system design

COURSE OUTCOME:

On completion of the course, student will be able to –

1: Learn Design flow graphs and flow modeling.

2: Understand SoC modeling and interfacing.

3:Gain knowledge of SoC memory system design, embedded software and energy management techniques for SoC design, SoC prototyping, verification, testing and physical design.

4: Design, implement and test SoC.

5. Analyze, integrate, and evaluate IP cores within a system-on-chip design flow using FPGA prototypes.

COURSE CONTENTS

UNIT-I	Basics of SoC	09Hrs

Basic Concepts: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSMD data-path, simulation and RTL synthesis, language mapping for FSMD.

UNIT-II	Micro-programmed Architectures	09Hrs

Micro-programmed Architectures : limitations of FSM , Micro-programmed : control, encoding , data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining , General

purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code, System on Chip, concept, design principles , portable multimedia system, SOCmodelling, hardware/software interfaces , synchronization schemes, memory mapped Interfaces , coprocessor interfaces, coprocessor control shell design, data and control design, Programmer's model

UNIT-III	RTL Simulation	09Hrs

RTL intent : Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.

UNIT-IV	SoC Design	09Hrs

Research topics in SOC design: A SOC controller for digital still camera, multimedia IP development image and video CODECS, SoC memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.

UNIT-V	IP based system design	09Hrs

IP based system design: Introduction to IP Based design, Types of IP, IP across design hierarchy,
IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.

LEARNING RESOURCES :

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer Publications.
2. Sanjay Churiwala, SapanGarg , "Principles of VLSI RTL Design A Practical Guide", Springer Publications.
3. Youn-Long Steve Lin, "Essential Issues in SOC Design, Designing Complex Systems-onChip", Springer Publications.
4. Wayne Wolf, "Modern VLSI Design Systems on Chip", Pearson Education.
4. Rajanish K. Kamat, Santhosh A. Shinde, Vinod G. Shelake, "Unleash the System On Chip using FPGAs and Handel C", Springer Publications.

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PCC-552-VLD: EMBEDDED TECHNOLOGIES and IoT

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To give insight to various platforms needed for Embedded Technologies and IoT.
2. To expose students to the usage of protocol standardization in Embedded Technologies and it's selection to various applications.
3. To Understand the fundamental of sensors and actuators along with the basic concepts of an IoT and how to design IoT based applications.

COURSE OUTCOME:

On completion of the course, student will be able to –

1. Understand various Embedded platforms and IoT platforms.
2. Comprehend the operation of different buses and protocols.
3. Interpret IoT architecture design aspects and its analyze concepts.
4. Develop design skills in industrial IoT.
5. Provide suitable solution for specific application and illustrate the technologies of IoT using suitable case studies.

Prerequisite Courses : Embedded System and analog circuits

COURSE CONTENTS

UNIT-I	ARM, Raspberry Pi Microcontroller	09Hrs

Basics of Raspberry Pi **(**RPi) board, Features and architecture, pin configurations, Installing OS on RPi, connecting to network, Programming languages with examples, Various interfaces e.g. I2C, UART, SPI, CAN. Node MCU ESP8266 Pin configuration, Station, AP, ST-AP modes, NodeMCU as web server, posting sensor data to gateway.

UNIT-II	Buses and Protocols	09Hrs

CAN Bus: Features and applications, CAN Frame, sequence of transmitting and receiving data on CAN Bus. Ethernet and USB Bus: Features and applications.Protocols: PHY/MAC Layer (3GPP MTC, IEEE 802.11, IEEE 802.15), Bluetooth Low Energy, Zigbee Smart Energy, Network Layer-IPv4, IPv6, 6LoWPAN, Transport Layer (TCP, MPTCP, UDP) Session Layer HTTP, CoAP, XMPP, AMQP, MQTT

UNIT-III	IoT Fundamentals	09Hrs

IoT Architecture and Design Concepts: IoT – An architectural overview, Design Principles and capabilities, M2M & IOT Technology Fundamentals- End Devices and gateways, Local and wide area networking, Challenges Associated with IoT, Cloud Platforms for IoT. Sensors: Different types of sensors and Actuators, Working, Networking Basics, RFID Principals and components, Wireless Sensor Networks, Physical Design of an IoT, Logical design of IoT Communication Models, Communication API's, Concept of IoE, Difference between IoT and IoE.

UNIT-IV	Industrial IoT	09Hrs

Introduction, Key Industrial IOT (IIoT) technologies, Catalysts, and precursors of IIoT, Innovation and the IIoT, Applications of IIoT Examples: Healthcare, Oil and Gas Industry, Logistics and the Industrial Internet, Retail applications, IoT innovations and design methodologies.

UNIT-V	IoT Applications	09Hrs

Applications: Smart Environment: Forest Fire Detection, Air Pollution, Smart Cities: Parking, Structural Health, Noise Urban maps, Smart Metering: Smart Grid, Tank level, Photovoltaic Installations, Health: Fall Detection, Medical Fridges, Sportsmen Care, Patients Surveillance.

LEARNING RESOURCES :

Text Books:

1. Olivier Hersent, David Boswarthick, and Omar Elloumi, "The Internet of Things: Key Applications and Protocols", 2 nd Edition, Wiley Publications.
2. Arshdeep Bahga and Vijay Madisetti , "Internet of Things: A Hands-On Approach", Orient Blackswan Private Limited - New Delhi; First Edition (1 January 2015).
3. Simon Monk , "Programming Raspberry Pi", McGraw Hill TAB; 2nd edition (16 November 2015).

Reference Books:

1. Andrew Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide – Designing and Optimizing System Software", ELSEVIER

2. Dr. Ovidiu Vermesan, Dr. Peter Friess, “Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems”, River Publishers Series
3. Rajesh Singh, “Internet of Things with Raspberry Pi and Arduino”, CRC Press 2020.

Laboratory Experiments:

1. IoT based stepper motor/ DC motor control using Raspberry-Pi
2. To interface sensors and actuators with Arduino/Raspberry-pi
3. To use MQTT/ CoAP protocol and send sensor data to cloud using Raspberry-Pi/ ESP8266.
4. To prepare IoT based small project implementation on the topics based on small problem statements of the fields like smart home (Home Automation) etc. This project can be built on any IoT simulation platform like Tinkercad, Cooja etc.

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PCC-553-VLD: RFIC DESIGN

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To study the various impedance matching techniques used in RF circuit design.
2. To understand the functional design aspects of LNAs, Mixers, PLLs and VCOs.
3. To understand frequency synthesis
4. To provide the knowledge of PLL architectures and building blocks
5. To introduce RF transceiver architectures and system-level design

COURSE OUTCOME:

On completion of the course, student will be able to:

1: Understand the principles of operation of an RF receiver front end

2: Design and apply constraints for LNAs, Mixers and frequency synthesizers

3: Analyze and design different types of oscillators, perform noise analysis.

4: Design PLL.

5: Evaluate and compare RF transceiver architectures and assess key performance parameters for wireless front-end design

COURSE CONTENTS

UNIT-I	RF Power Amplifiers Design	09Hrs

Definition of ‘Q’, Series Parallel Transformations of Lossy Circuits, Impedance Matching Using ‘L’,‘Pi’ and T Networks, Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers, Noise Characteristics of MOS Devices, Design of CG LNA and Inductor Degenerated LNAs. Principles of RF Power Amplifiers Design

UNIT-II	Mixer and principles of working	09Hrs

Qualitative Description of the Gilbert Mixer - Conversion Gain, and Distortion and Noise , Analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - a Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended

Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.		
UNIT-III	Oscillators and Types	09Hrs
LC Oscillators, Voltage Controlled Oscillators, Ring Oscillators, Delay Cells, Tuning Range in Ring Oscillators, Tuning in LC Oscillators, Tuning Sensitivity, Phase Noise in Oscillators, Sources of Phase Noise		
UNIT-IV	Phase Locked Loops	09Hrs
Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer		
UNIT-V	RF Transceiver Architectures and System-Level Design	09Hrs
Heterodyne and Homodyne Receiver Architectures, Image Rejection and I/Q Mismatch Issues, Direct Conversion & Low-IF Architectures, Transmitter Design Considerations (Linearity, Efficiency, Spectral Purity), System-Level Noise Figure, Linearity (IIP3, P1dB), Dynamic Range, Power Consumption Trade-offs in RFICs, Case Study: RF Front-end for Wireless Standards (e.g., LTE/5G, WLAN, Bluetooth)		
LEARNING RESOURCES :		
1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998 2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002 3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mcgraw-Hill, 1999 4. Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001 5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003		

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PCC-554-VLD: DESIGN LAB-II

Teaching Scheme	Credits	Examination Scheme
Theory : 04 Hours/Week	04	TW Marks: 25 Marks OR Marks : 25 Marks

COURSE OBJECTIVE:

1. To integrate IP cores and design subsystems for SoC applications
2. To expose students to FPGA prototyping and real-time testing
3. To design and analyze RF building blocks like LNA, Mixer, VCO, and PA
4. To provide hands-on experience using CAD tools for RFIC design.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Integrate hardware/software co-design in SoC.
2. Demonstrate FPGA implementation of SoC subsystems
3. Analyze key RF performance metrics (S-parameters, NF, IP3, gain, etc.).
4. Design and simulate RF front-end circuits using CAD tools.

LABORATORY EXPERIMENTS (*Any 4)

1. Design of an Arithmetic Logic Unit (ALU) as an IP block.
2. Simulation of simple digital modules using **HDL (Verilog/VHDL) and SoC tool flow**
3. Implementing designed SoC on FPGA board
4. Design of Low Noise Amplifier (LNA) – gain and noise analysis
5. Mini Project – RF front-end transceiver chain integration (LNA + Mixer + VCO)
6. Mini Project – e.g., Smart sensor interface system, embedded controller on FPGA.

LEARNING RESOURCES:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mcgraw-Hill, 1999
4. Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001

5. Thomas H.Lee, “The Design of CMOS Radio –Frequency Integrated Circuits’, Cambridge University Press ,2003

6. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer Publications.

7. Sanjay Churiwala, SapanGarg , “Principles of VLSI RTL Design A Practical Guide”, Springer Publications.

8. Youn-Long Steve Lin, “Essential Issues in SOC Design, Designing Complex Systems-onChip”, Springer Publications.

9. Wayne Wolf, “Modern VLSI Design Systems on Chip”, Pearson Education.

10. Rajanish K. Kamat, Santhosh A. Shinde, Vinod G. Shelake, “Unleash the System On Chip using FPGAs and Handel C”, Springer Publications.

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PEC-561A-VLD: Elective II : MACHINE LEARNING

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. Introduce fundamental Machine Learning concepts and their applications in real-world problems.
2. Implement regression and classification models to solve engineering problems
3. Apply clustering and dimensionality reduction techniques to unlabeled data.
4. Optimize datasets through preprocessing and feature selection for Machine Learning pipelines.
5. Combine models and validate performance for robust predictions.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Compare Machine Learning paradigms for real time applications
2. Design regression models for predictive tasks and classification models (SVM, decision trees) for signal/label prediction.
3. Develop clustering models (K-Means, DBSCAN) and PCA-based solutions for defect detection or customer segmentation.
4. Construct feature engineering pipelines (scaling, encoding, and selection) to improve model performance in VLSI/telecom datasets.
5. Implement ensemble techniques like Random Forest, XGBoost and statistical tests like t-test to enhance accuracy in IC testing or power grid stability.

Prerequisite Courses : Engineering Mathematics (Linear Algebra, Probability & Statistics, Calculus), Digital signal processing ,Data Structures and Algorithms

COURSE CONTENTS

UNIT-I	Introduction to Machine Learning	07Hrs

Introduction, Definition and motivation, History and evolution of Machine learning, types : Supervised, Unsupervised, Semi-supervised, Reinforcement, Machine Learning Models: Geometric, Probabilistic, Logical, and Parametricvs. Non-parametric, Applications of Machine

Learning in Signal processing, speech recognition, image processing, Wireless communications		
UNIT-II	Supervised Machine Learning	07Hrs
Introduction to Supervised Learning, Types of Supervised Problems, Regression Models: Linear Regression, Types of Linear Regression, cost function, gradient descent of linear regression, Evaluation Metrics for Linear Regression Classification Models: Logistic 1. Naive Bayes algorithm 2.KNN algorithm 3.Support Vector Machine (SVM).		
UNIT-III	Unsupervised Machine Learning	07Hrs
Introduction, Types of Unsupervised Learning: Clustering, Association Rule Learning, Dimensionality Reduction, K-means Clustering algorithm, Evaluation: Elbow method, Silhouette score, Density-Based Methods, Dimensionality Reduction Techniques, Principal Component Analysis (PCA), Apriori		
UNIT-IV	Feature Engineering	07Hrs
Importance of feature engineering in Machine Learning pipeline, Handling missing values, outliers, Encoding: Label, One-Hot, Ordinal, Target Scaling: Min-Max, Standardization, Normalization, Feature selection: Filter (Chi-square), Wrapper (RFE), Embedded (Lasso)		
UNIT-V	Ensemble Learning and Model Evaluation	07Hrs
Introduction to Ensembles, Need of Ensemble Learning , Basic Ensemble Learning Techniques: Voting (Hard/Soft), Advanced Ensemble Learning Techniques: Bagging (Random Forest), Boosting (AdaBoost, XGBoost), Stacking, Cross-validation: Hold-out, K-Fold, LOOCV, Model comparison using t-test, McNemar's test, Hyperparameter tuning (Grid Search, Random Search)		
LEARNING RESOURCES :		
Text Books:		
1. Ethem Alpaydin, "Introduction to Machine Learning", Publisher: The MIT Press,2014 2. Peter Flach, "Machine Learning: The Art and Science of Algorithms that Make Sense of Data", Cambridge University Press, Edition 2012		
ReferenceBooks:		
1. Ian H Witten, Eibe Frank, Mark A Hall, "Data Mining, Practical Machine Learning Tools and Techniques", Elsevier, 3rd Edition 2. Jiawei Han, Micheline Kamber, and Jian Pie, "Data Mining: Concepts and Techniques",		

Elsevier Publishers Third Edition, ISBN: 9780123814791, 9780123814807

3. Shalev-Shwartz, Shai, and Shai Ben-David, “Understanding machine learning: From theory to algorithms”, Cambridge university press, 2014
4. McKinney, “Python for Data Analysis O' Reilly media, ISBN : 978-1-449- 31979-3

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PEC-561B -VLD-: Elective II - Mixed Signal IC Design

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

- To understand the fundamentals of analog and discrete-time signals, signal conversion, and the design considerations of mixed-signal systems.
- To study various DAC and ADC architectures and their principles of operation.
- To develop modeling techniques for data converters with emphasis on sampling, reconstruction, and quantization noise.
- To explore performance parameters of data converters such as SNR, ENOB, and dynamic range.
- To understand advanced performance improvement techniques in data converters using spectral analysis, dithering, and digital filters.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Analyze ADC/DAC specifications and apply mixed-signal layout techniques for reliable converter design.
2. Compare and select suitable ADC/DAC architectures for given application requirements.
3. Model converter behavior and evaluate the impact of sampling and quantization noise on system performance.
4. Assess data converter performance considering noise, distortion, and jitter effects.
5. Apply dithering and digital filtering techniques to enhance ADC/DAC performance.

COURSE CONTENTS

UNIT-I	Analog-to-Digital Conversion and Mixed-Signal Design	07 Hrs

Analog versus discrete time signals, Converting analog signal to digital signal, Sample and hold characteristics, DAC specifications, ADC specifications, Mixed signal layout issues: floor planning, power supply and grounding issues, fully differential design/ matching, guard rings, shielding, interconnect considerations

UNIT-II	Data Converter Design: DACs and ADCs	07 Hrs

DAC architectures: Resistor string, R-2R ladder networks, Current steering, Charge-scaling, Pipeline. ADC architectures: Flash, Pipeline, Dual slope, Successive approximation, Oversampling ADC		
UNIT-III	Modeling and Analysis of Data Converters	07 Hrs
Data converter modeling: Sampling and aliasing: A modeling approach, Impulse sampling, AAF and RCF, Time domain description of reconstruction, The sample and hold, S/H spectral response, Circuit concerns for implementing S/H. Quantization noise, RMS quantization noise voltage		
UNIT-IV	Data Converter Signal Quality	07 Hrs
Data converter SNR: Effective number of bits, Signal to noise plus distortion ratio, Spurious free dynamic range, dynamic range, SNR & SNDR, Clock jitter, Averaging to improve SNR		
UNIT-V	Data Converter Design	07 Hrs
Spectral density view, Jitter and averaging, Relaxed requirements on AAF, Data converter linearity requirements, Adding noise dither to ADC input, Decimating filters for ADC, Decimating filters for ADCs, Interpolating filters for DACs.		
LEARNING RESOURCES :		
1. Baker R J, “CMOS: Mixed Signal Circuit Design”, Second edition, Wiley IEEE Press Publications. 2. Baker R J, “CMOS: Circuit Design, Layout and Simulation”, Second edition, Wiley IEEE Press Publications. 3. Allen, Phillip E., Holberg, Douglus R., “CMOS Analog Circuit Design”, Oxford University Press Publications.		

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PEC-561C-VLD: ELECTIVE-II-Real Time Operating Systems

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To learn software architectures, programming concepts, and software development processes for embedded systems.
2. To understand fundamental operating system concepts including processes, memory, I/O, files, and security.
3. To study different operating system structures and their design approaches.
   To understand real-time operating system concepts and kernel structures for embedded applications.
4. To explore Linux/RT Linux features, commands, shell/system programming, and POSIX threads

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Design and implement efficient embedded programs using C/C++ with optimized memory and data structures.
2. Analyze and apply operating system mechanisms for process management, memory handling, and secure file operations.
3. Differentiate between monolithic, layered, virtual machine, exokernel, and client-server OS models.
4. Implement task management, synchronization, and communication in a real-time operating system.
5. Develop applications using Linux/RT Linux utilities and implement multitasking with POSIX threads.

COURSE CONTENTS

UNIT-I	Embedded Software Architectures and	07 Hrs

	Programming	
Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model		
UNIT-II	Operating System Concepts and Fundamentals	07 Hrs
Operating System Concepts, Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts.		
UNIT-III	Operating System Structures and Models	07 Hrs
Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model		
UNIT-IV	Real-Time Operating System Fundamentals	07 Hrs
Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization		
UNIT-V	Linux	07 Hrs
Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads		

Learning Resources

Text Books:

1. Labrossy J. J, Lawrence, "µC/OS-II, The Real Time Kernel", R & D Publication.
2. Dr Prasad K V K K, "Embedded Real Time Systems: Concepts, Design & Programming", Dreamtech Publication.
3. Simon D. E, "An Embedded Software Primer", Pearson education.
4. Tanenbaum A S, "Modern Operating Systems", Prentice Hall.
5. Raj Kamal, "Embedded Systems Architecture, Programming and design", Tata Mc- Graw-Hill.

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PEC-561D-VLD: ELECTIVE-II-
DIGITAL IMAGE PROCESSING AND PATTERN RECOGNITION

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

- To introduce the fundamentals of digital image processing, image formation, sampling, quantization, and pixel relationships.
- To study spatial and frequency domain techniques for image enhancement and filtering.
- To understand image restoration techniques, wavelet transforms, and compression concepts.
- To learn information theory principles and image/video compression standards.
- To introduce the fundamentals of pattern recognition and classification techniques.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Explain image formation concepts and apply sampling, quantization, and pixel relationships in image analysis.
2. Implement image enhancement methods using spatial and frequency domain filtering.
3. Restore degraded images and apply wavelet-based methods and coding techniques for image compression.
4. Apply compression algorithms and standards such as JPEG, JPEG2000, and MPEG for efficient image/video storage and transmission.
5. Design a basic pattern recognition system using statistical methods, neural networks, and wavelet transforms.

COURSE CONTENTS

UNIT-I	Introduction of Digital Image Processing	07 Hrs

Digital Image Processing, Components of an Image Processing system, Applications. Human Eye and Image Formation; Sampling and Quantization, Basic Relationship among pixels- neighbour, connectivity, regions, boundaries, distance measures

UNIT-II	Image Enhancement	07 Hrs

Spatial Domain, Gray Level transformations, Histogram, Arithmetic/Logical Operations, Spatial filtering, Smoothing & Sharpening Spatial Filters; Frequency Domain- 2-D Fourier transform, Smoothing and Sharpening Frequency Domain Filtering; Convolution and Correlation Theorems		
UNIT-III	Image Restoration	07 Hrs
Inverse filtering, Wiener filtering; Wavelets- Discrete and Continuous, Wavelet Transform, Wavelet Transform in 2-D; Image Compression: Redundancies- Coding, Interpixel, Psycho visual; Fidelity, Source and Channel Encoding		
UNIT-IV	Image and Video Compression Techniques	07 Hrs
Elements of Information Theory; Loss Less and Lossy Compression; Run length coding, Differential encoding, DCT, Vector quantization, entropy coding, LZW coding; Image Compression Standards- JPEG, JPEG 2000, MPEG; Video compression		
UNIT-V	Pattern Recognition	07 Hrs
Introduction to pattern recognition, Pattern Recognition Methods, Pattern Recognition System Design, Statistical Pattern recognition – Classification, Principle, Classifier learning, Neural networks for pattern classification. The Wavelet Transform, Discrete-time orthogonal wavelets, continuous time orthogonal wavelet basis		
LEARNING RESOURCES:		
1. Fundamentals of Digital Image processing by A. K. Jain, Pearson Education. 2. Digital Image Processing by R. C. Gonzalez and R. E. Woods, Pearson Education. 3. Digital Image Processing using MATLAB by R. C. Gonzalez , R. E. Woods and S. L Eddins, Pearson Education. 4. Digital Image Processing and Analysis by Chanda and Mazumdar, PHI. 5. Multirate Digital Signal Processing by N.J. Fliege, John Wiley and Sons		

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PEC-562 A- VLD: Elective III - CLOUD ARCHITECTURE PROTOCOLS

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

The course aims to:

1. Define core cloud architecture principles using standardized models (NIST, SPI).
2. Analyze network protocol mechanics, including encapsulation systems and datacenter topologies.
3. Evaluate security frameworks using cryptographic protocols and identity management algebras.

COURSE OUTCOME:

Upon successful completion of this course, students will be able to:

1. Classify cloud service/deployment models using NIST taxonomies and deconstruct virtualization architectures.
2. Analyze encapsulation protocols and data center fabrics using routing algebras and congestion control formalisms.
3. Analyze the components of a virtualized data center and review the performance of Data archiving solutions.
4. Implement /identity cryptographic protocols via state-machine models and Zero Trust policy algebras.
5. Quantify system resilience using queueing theory, failure distributions and resource optimization heuristics.

COURSE CONTENTS

UNIT-I	CLOUD ONTOLOGY & ARCHITECTURAL FRAMEWORKS	09 Hrs

Foundational Models: NIST essential characteristics, SPI service model taxonomy, resource abstraction layers. Deployment Topologies: Public, Private and Hybrid structural patterns, community cloud governance frameworks. Virtualization Theory: Hypervisor architectures (Bare-metal/Hosted), container isolation formalisms, docker basics and architecture.

UNIT-II	NETWORK VIRTUALIZATION & PROTOCOL ARCHITECTURES	07 Hrs

Encapsulation Systems: VXLAN/Geneve header structures, NVGRE protocol mechanics, virtual switching paradigms. Data Center Fabrics: BGP-EVPN control plane theory, Clos topology mathematics,

spine-leaf routing algebras. Transport Layer Theory: TCP congestion control formalisms, QoS traffic shaping models, packet scheduling algorithms.

UNIT-III	STORAGE NETWORKS	08 Hrs

Storage network design considerations: NAS and FC SANs, hybrid storage networking technologies (iSCSI, FCIP, FCoE), design for storage virtualization in cloud computing, host system design considerations. Replications in NAS and SAN environments. Data archiving solutions, analyzing compliance and archiving design considerations.

UNIT-IV	SECURITY PROTOCOLS & CRYPTOGRAPHIC FRAMEWORKS	07 Hrs

Identity Systems: SAML 2.0 assertion flows, OAuth 2.0 grant type formalisms, RBAC/ABAC policy algebras. Cryptographic Systems: TLS 1.3 handshake state machine, AES-GCM mode operations, PKI trust hierarchies. Network Security Models: Zero Trust formal architectures, IPsec/IKEv2 tunneling protocols, firewall policy verification.

UNIT-V	SCALABILITY & RELIABILITY THEORY	07 Hrs

Elasticity Frameworks: Autoscaling hysteresis models, M/M/c queueing systems, horizontal scaling proofs. Failure Engineering: Weibull failure distributions, RTO/RPO calculus, chaos engineering principles. Cost Governance Ontologies: TCO analytical frameworks, bin packing optimization, cloud governance taxonomies.

LEARNING RESOURCES:

Text Books:

1. T. Erl et al., Cloud Computing: Concepts, Technology & Architecture. Upper Saddle River, NJ: Prentice Hall, 2013.
2. D. Dutt, Cloud Native Data Center Networking. Sebastopol, CA: O'Reilly Media, 2019.
3. B. Beyer et al., Site Reliability Engineering: How Google Runs Production Systems. Sebastopol, CA: O'Reilly Media, 2016.
4. C. Wu and R. Buyya, Cloud Data Centers and Cost Modeling: A Complete Guide To Planning, Designing and Building a Cloud Data Center. Cambridge, MA: Morgan Kaufmann, 2015.

Reference Books:

1. R. Mather et al., Cloud Security: A Comprehensive Guide to Secure Cloud Computing. Hoboken, NJ: Wiley, 2010.

2. P. Mell and T. Grance, The NIST Definition of Cloud Computing, NIST SP 800-145. Gaithersburg, MD: National Institute of Standards and Technology, 2011.
3. A. Azodolmolky, Cloud Networking: Understanding Cloud-Based Data Center Networks. Waltham, MA: Morgan Kaufmann, 2014.

SWAYAM/ MOOC / eBOOKS

1. Cloud computing By Prof. Soumya Kanti Ghosh, IIT Kharagpur
https://onlinecourses.nptel.ac.in/noc21_cs14/preview
2. Advanced Computer Networks, By Prof. Neminath Hubballi, Prof. Sameer G Kulkarni IIT Indore, IIT Gandhi nagar
https://onlinecourses.nptel.ac.in/noc25_cs02/preview
3. Cloud Computing and Distributed Systems By Prof. Rajiv Misra IIT Patna
https://onlinecourses.nptel.ac.in/noc21_cs15/preview

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PEC-521B-VLD: ELECTIVE-I- FUZZY MATHEMATICS

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. Understand the fundamental concepts and properties of fuzzy sets and fuzzy logic systems.
2. Explore mathematical operations and structures involved in fuzzy set theory.
3. Analyze the algebraic operations and relationships between fuzzy sets and fuzzy relations.
4. Apply fuzzy logic principles in mathematical modeling using logical gates and fuzzy subgroups.
5. Develop skills to use fuzzy logic in real-world problem-solving contexts.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Explain the basic concepts of fuzzy subsets, partial ordering, lattice theory, and Boolean algebras.
2. Perform fundamental operations on fuzzy sets including union, intersection, and complement.
3. Apply algebraic sum and product operations on fuzzy subsets.
4. Understand the use of logic connectives in fuzzy logic and their implications.
5. Illustrate fuzzy logic using logic gates.

COURSE CONTENTS

UNIT-I	INTRODUCTION TO FUZZY LOGIC	07Hrs
Introduction to Fuzzy subsets and its properties, Partially ordered sets, Lattice and Boolean Algebras, L fuzzy sets.		
UNIT-II	OPERATIONS AND PROPERTIES OF FUZZY SET	07Hrs
Operations on fuzzy sets, Disjunctive sum, levels sets and properties of fuzzy subsets of a set.		
UNIT-III	ALGEBRIC OPERATIONS ON FUZZY SET	07Hrs
Algebraic product and sum of two fuzzy subsets, properties satisfied by addition and product Cartesian product of fuzzy subsets.		

UNIT-IV	ALGEBRA OF FUZZY RELATIONS	07Hrs
Fuzzy Relations, Algebra of fuzzy relations, Properties of fuzzy relations, Logic Connectives.		
UNIT-V	FUZZY LOGIC USING GATES	07Hrs
Connectives – Exclusive or, NAND, NOR, Fuzzy Logic fuzzy subgroup & Lattice of Fuzzy Sub Group homomorphic image and Pre- image of subgroups.		

LEARNING RESOURCES:

1. S.Nanda and N.R.Das "Fuzzy Mathematical concepts, Narosa Publishing House, New Delhi.
2. Fuzzy Logic with Engineering Applications, Second Edition, Wiley Publications, Timothy J.Ross.
3. Fuzzy Set Theory and Its Applications, Fourth Edition, Yes Dee Publishing Pvt. Ltd., Springer, H.-J. Zimmermann.

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PEC-562C- VLD: ELECTIVE III - RENEWABLE ENERGY STUDIES

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. Understand the classification and availability of different energy sources, including renewable and non-renewable forms.
2. Gain insights into the fundamentals and technologies behind various non-conventional energy sources such as solar, wind, biomass, and ocean energy.
3. Study wind energy systems and evaluate the design and operation of wind turbines.
4. Explore biomass energy conversion methods and applications, including biogas and gasification technologies.
5. Examine additional renewable technologies such as geothermal, hydrogen energy, fuel cells, MHD, and ocean-based systems.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Differentiate between conventional and non-conventional energy sources.
2. Explain solar radiation concepts and apply solar energy data for energy estimation.
3. Describe wind energy systems, including types of turbines and site considerations.
4. Analyze biomass energy technologies and evaluate their operational effectiveness.
5. Evaluate the principles, benefits, and limitations of alternative renewable sources such as geothermal, hydrogen, MHD, OTEC, tidal, and wave energy.

COURSE CONTENTS

UNIT-I	ENERGY SOURCES & AVAILABILITY	07 Hrs

Conventional, non-conventional, renewable, non-renewable sources of energy, prospects, perspectives, & advantages. Introduction to different types of non- conventional source of energy: solar, wind, biomass, Ocean Thermal Energy Conversion (OTEC), geothermal, hydrogen energy, fuel cells, thermionic power conversion, thermoelectric power conversion.

UNIT-II	SOLAR ENERGY	07 Hrs

Solar constant, solar radiation geometry, local solar time, day length, solar radiation measurement, radiation on inclined surface, solar radiation data, & solar charts.		
UNIT-III	WIND ENERGY	07 Hrs
Wind as a source of energy, Characteristics of wind, wind data. Horizontal & vertical axis wind turbines.		
UNIT-IV	BIOMASS ENERGY	07 Hrs
Introduction to biomass, biofuels & their heat content, biomass conversion technologies. Aerobic & anaerobic digester, Factors affecting bio-digestion, biogas plants–types. Biomass gasification: Gasifier types, direct thermal application of gasifiers. Advantages & problems in development of gasifiers.		
UNIT-IV	OTHER RENEWABLE ENERGY SOURCES	07 Hrs
Geothermal Energy: Status & estimates, geothermal resources, geothermal systems & their characteristics. Hydrogen energy. Fuel Cells: Principle & classification, types, conversion, efficiency, polarization, & advantages. Magneto Hydro Dynamic.		

LEARNING RESOURCES :

1. B. H. Khan, “Non-Conventional Energy Resources”.
2. Godfrey Boyle, “Renewable Energy”.
3. D. P. Kothari, K. C. Singhal, and Rakesh Ranjan, “Renewable Energy Sources and Emerging Technologies”.
4. S. P. Sukhatme and J. K. Nayak, “Solar Energy: Principles of Thermal Collection and Storage”.

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PEC-562 D- VLD: ELECTIVE III - DESIGN AND ANALYSIS OF ALGORITHMS

Teaching Scheme	Credits	Examination Scheme
Theory : 03 Hours/Week	03	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To demonstrate performance of algorithms with respect to time and space complexity.
2. To explain graph and tree traversals.
3. To explain the concepts greedy method and dynamic programming. Applying for several applications like knapsack problem, job sequencing with deadlines, and optimal binary search tree, TSP and so on respectively.
4. To Illustrate the methods of backtracking and branch bound techniques to solve the problems like n-queens' problem, graph coloring and TSP respectively.
5. To familiarize the concepts of deterministic and non-deterministic algorithms.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Identify various Time and Space complexities of various algorithms.
2. Understand Tree Traversal method and Greedy Algorithms.
3. Apply Dynamic Programming concept to solve various problems.
4. Apply Backtracking, Branch and Bound concept to solve various problems.
5. Implement different performance analysis methods for non -deterministic algorithms.

COURSE CONTENTS

UNIT-I	INTRODUCTION TO ALGORITHMS	07 Hrs

Algorithm, pseudo code for expressing algorithms, performance analysis-space complexity, time complexity, asymptotic notation- big (O) notation, omega notation, theta notation and little (o) notation, recurrences, probabilistic analysis, disjoint set operations, union and find algorithms.

UNIT-II	METHODS AND ANALYSIS	07 Hrs

DIVIDE AND CONQUER: General method, applications-analysis of binary search, quick sort, merge sort, AND OR Graphs.

GREEDY METHOD: General method, Applications-job sequencing with deadlines, Fractional

knapsack problem, minimum cost spanning trees, Single source shortest path problem.		
UNIT-III	ALGORITHM AND ANALYSIS	07 Hrs
GRAPHS: Breadth first search and traversal, Depth first search and traversal, Spanning trees, connected components and bi-connected components, Articulation points. DYNAMIC PROGRAMMING: General method, applications - optimal binary search trees, 0/1 knapsack problem, All pairs shortest path problem, Travelling sales person problem, Reliability design.		
UNIT-IV	BRANCH AND BOUND	07 Hrs
BACKTRACKING: General method, Applications- n-queen problem, Sum of subsets problem, Graph coloring and Hamiltonian cycles. BRANCH AND BOUND: General method, applications - travelling sales person problem, 0/1 knapsack problem- LC branch and bound solution, FIFO branch and bound solution.		
UNIT-V	PROBLEMS ON ALGORITHMS AND CLASSES	07 Hrs
NP-HARD AND NP-COMPLETE PROBLEMS: Basic concepts, non-deterministic algorithms, NP-hard and NP-complete classes, Cook ‘s theorem.		
LEARNING RESOURCES :		
1.Ellis Horowitz, Satraj Sahni, Rajasekharam , Fundamentals of Computer Algorithms, 2nd edition, University Press, New Delhi. 2. R. C. T. Lee, S. S. Tseng, R.C. Chang and T. Tsai (2006), Introduction to Design and Analysis of Algorithms A strategic approach, McGraw Hill, India. 3.Allen Weiss (2009), Data structures and Algorithm Analysis in C++, 2nd edition, Pearson education, New Delhi. 4. Aho, Ullman, Hopcroft (2009), Design and Analysis of algorithms, 2nd edition, Pearson education, New Delhi		

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Semester III

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RM-631-VLD: RESEARCH METHODOLOGY

Teaching Scheme	Credits	Examination Scheme
Theory : 05Hours/Week	05	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. Understand the philosophy of research in general
2. Understand basic concepts of research and its methodologies
3. Learn the methodology to conduct the Literature Survey
4. Acquaint with the tools, techniques, and processes of doing research
5. Learn the effective report writing skills and allied documentations
6. Become aware of the ethics in research, academic integrity and plagiarism

COURSE OUTCOME:

On completion of the course, student will be able to:

1. D**efine** research and **explain** its essential characteristics with examples from engineering and science fields
2. Identify and **apply** different types of research (basic, applied, qualitative, quantitative, exploratory, descriptive, etc.) to specific problems
3. **Analyze** the outcomes of research such as publications, patents, and technological contributions, and understand their societal and industrial impacts
4. **Apply** ANOVA and ANCOVA techniques for effective experimental data analysis and interpretation of results
5. **Understand** and **apply** the basics of Intellectual Property Rights (IPR) to safeguard innovative research and prevent unethical practices

Prerequisite Courses:

1. Familiarity with project-based learning (e.g., mini projects, seminars, undergraduate theses)
2. Knowledge of basic statistics (mean, median, variance, standard deviation, probability concepts)
3. Basic skills in technical writing (reports, presentations, documentation).

4. Sound fundamentals of the core engineering/science domain

COURSE CONTENTS		
UNIT-I	Definition and Characteristics of Research	12Hrs

Basic of Research: Definition; Concept of Construct, Postulate, Proposition, Thesis, Hypothesis, Law, Principle. Philosophy and validity of research. Objective of research. Various functions that de- scribe characteristics of research such as systematic, valid, verifiable, empirical and critical approach. Types - Pure and applied research. Descriptive and explanatory research. Qualitative and quantitative approaches.

Engineering Research: Why? Research Questions, Engineering Ethics, conclusive proof-what constitutes, A research project-Why take on?

Case Study : Code of Ethics, IEEE Code of Ethics, ACM Software Engineering Code of Ethics and Professional Practice, Code of Ethics especially covering Engineering discipline, various aspects- environment, sustainable outcomes, employer, general public, and Nation, Engineering Disasters

UNIT-II	Literature Search and Review	12Hrs

Literature Review, Types of review, Developing the objectives, Preparing the research design including sample Design, Sample size. Archival Literature, Why should engineers be ethical? Types of publications- Journal papers, conference papers, books, standards, patents, theses, trade magazine, newspaper article, infomercials, advertisement, Wikipedia & websites, Measures of research impact, publication cost.

Case Study : Engineering dictionary, Shodhganga, The Library of Congress, Research gate, Google Scholar, Bibliometrics, Citations, Impact Factor, h-index, I-index, plagiarism, copyright infringement

UNIT-III	Analysis of Variance and Covariance	12Hrs

Basic principle of Analysis of Variance, ANOVA Technique, Setting up Analysis of Variance Table, short-cut method for one-way ANOVA, Coding method, Two-way ANOVA, ANOVA in Latin-square design, analysis of co-variance (ANCOVA), assumptions in ANCOVA. Academic Ethics: Plagiarism, exposure on anti-plagiarism tools.

UNIT-IV	Technical Writing and IPR	12Hrs

Academic writing, sources of information, assessment of quality of journals and articles, writing scientific report, structure and component of research report, types of report – technical reports and thesis, SCOPUS Index, citations, search engines beyond google, impact factor, H-Index. IPR: What is IPR?, importance of patents, types of IPR, process of

patent.

UNIT-V	Outcome of Research and Research Presentation	12Hrs

Relevance, interest, available data, choice of data, Analysis of data, Generalization and interpretation of analysis, Preparation of the Report on conclusions reached, Testing validity of research outcomes, Suggestions and recommendations, identifying future scope.

Research presentation: Introduction, Standard terms, Standard research methods and experimental techniques, Paper title and keywords, Writing an abstract, Paper presentation and review, Conference presentations, Poster presentations, IPR, Copyright, Patents.

Case Study: Intellectual Property India- services, InPASS - Indian Patent Advanced Search System,

US patent, IEEE / ACM Paper templates

LEARNING RESOURCES :

Text Book:

1. Dawson, Catherine, 2002, Practical Research Methods, New Delhi, UBS Publishers' Distributors.
2. Kothari, C.R.,1985, Research Methodology-Methods and Techniques, New Delhi, Wiley Eastern Limited.
3. Kumar, Ranjit, 2005, Research Methodology-A Step-by-Step Guide for Beginners, (2nd.ed), Sin- gapore, Pearson Education.
4. Neeraj Pandey, Intellectual Property Rights ,1st Edition, PHI
5. Shrivastava, Shenoy& Sharma, Quantitative Techniques for Managerial Decisions, Wiley

Reference Book:

1. Goode W J &Hatt P K, Methods in Social Research, McGraw Hill
2. Basic Computer Science and Communication Engineering – R. Rajaram (SCITECH)

NPTEL/SWAYM/MOOC:

1. https://www.youtube.com/playlist?list=PLm-zueI9b64QGMcfn5Ckv_8W5Z1d3vMBY
2. https://onlinecourses.swayam2.ac.in/cec20_hs17/preview
3. https://onlinecourses.nptel.ac.in/noc23_ge36/preview

Practical Assignments / Mini Project Problem Statements		
Sr.	**Title**	**Objectives**
1	Problem Identification Exercise	Identify and clearly define a real-world research problem in your engineering discipline.
2	Literature Review Report	Conduct a detailed literature survey (minimum 30 research papers) and summarize gaps in existing research.
3	Research Proposal Drafting	Prepare a structured research proposal including problem statement, objectives, scope, and methodology.
4	Hypothesis Formulation	Develop testable hypotheses based on selected research problems.
5	Design of Experiment	Design a detailed experimental plan or simulation for validating hypotheses.
6	Sampling Techniques	Select and justify a sampling method for data collection in your project.
7	Data Collection Tools Development	Design a survey questionnaire or sensor-based data collection method.
8	Statistical Data Analysis	Perform statistical analysis (ANOVA, regression, t-tests) on sample data.
9	Research Paper Writing	Draft a full research paper based on hypothetical or preliminary data.
10	Research Ethics and Plagiarism Check	Analyze ethical aspects and conduct a plagiarism check for your paper.

Mini Project statement list for Research Methodology (ANY ONE)		
Sr.	**Project Title**	**Description/Deliverable**
1	AI-based Systematic Literature Review Tool	Build a tool that automates screening and organizing research papers.
2	Comparison of Research Methodologies	Compare qualitative vs. quantitative methods through case studies.
3	Development of a Research Gap Identification Model	Create an algorithm that detects research gaps from published articles.
4	Design of a Predictive Analytics Model	Design a model that predicts the future trend of research in a selected field.
5	Big Data Analysis for Research Trends	Analyze publication data from Scopus/IEEE/Google Scholar to identify top emerging topics.
6	AI-based Systematic Literature Review Tool	Build a tool that automates screening and organizing research papers.

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OJT-641-VLD: INTERNSHIP/ON JOB TRAINING (IN/OJT)

Teaching Scheme	Credits	Examination Scheme
Theory : 05Hours/Week	05	CCE* Marks: 50 Marks End Semester (Th) : 50 Marks

COURSE OBJECTIVE:

1. To put theory into practice. And expand thinking and broaden the knowledge and skills acquired through course work in the field.
2. To relate to, interact with, and learn from current professionals in the field.
3. To understand and adhere to professional standards in the field.
4. To gain insight to professional communication including meetings, memos, reading, writing, public speaking, research, client interaction, input of ideas, and confidentiality.
5. To develop the initiative and motivation to be a self-starter and work independently.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. **Gain** practical experience within industry in which the internship is done.
2. **Acquire** knowledge of the industry in which the internship is done.
3. **Apply** knowledge and skills learned to classroom work.
4. **Develop** and refine oral and written communication skills.
5. **Acquire** the knowledge of administration, marketing, finance and economics.

COURSE DESCRIPTION

1. Internship/On Job Training provide students the opportunity of hands-on experience that includes personal training, time and stress management, interactive skills, presentations, budgeting, marketing, liability and risk management, paperwork, equipment ordering, maintenance, responding to emergencies etc.
2. An internship is the phase of time for students when they are trained for their skills, they are good at, and it gives them a chance to apply their knowledge practically in industries

3. The internship can be carried out in any industry/R&D Organization/Research Institute/Institute of national repute/R&D Centre of Parent Institute.

4. The Department/college shall nominate a faculty to facilitate, guide and supervise students under internship.

GUIDELINES

- Purpose: Internships are designed to bridge the gap between academic learning and industry practice. They aim to provide hands-on experience, expose students to the industrial environment, develop technical and soft skills (communication, teamwork, problem-solving), and help in career exploration

- Internship Duration and Academic Credentials

1.Student can take internship work in the form of Online/Offline mode from any of the Industry / Government Organization Internship Programs approved by SPPU/AICTE/UGC portals

2.A intern is expected to spend 10 - 12 hours per week on Internship, Training will result in about 160-170 hours of total internship duration.

3.The minimum requirement regarding Internship duration should not be below 8 weeks

- Type of Internship

1. Industry/Government Organization Internship: Working directly with a company or government body.

2. Research Internship: Focused on research projects, often in collaboration with academic institutions or R&D labs.

3. Innovation/Entrepreneurship: Working on developing new products, processes, or even starting a venture.

4. Social Internship: Engaging in community-based projects.

- Assessment Details (TW and Practical)

1.Term work for 100 marks

2. A daily log submitted by the student and a work log signed by the office HoDs where the student has interned will be considered towards the TW marking.

- Indicative list of areas for OJT

1.Trade and Agriculture

2.Economy & Banking Financial Services and Insurance

3.Logistics, Automotive & Capital Goods

4.Fast Moving Consumer Goods & Retail

5.Information Technology/Information Technology Enabled Services & Electronics

6.Handcraft, Art, Design & Music

7.Healthcare & Life Science

8.Sports, Wellness and Physical Education

9.Tourism & Hospitality

10. Digitization & Emerging Technologies (Internet of Things / Artificial Intelligence / Machine Learning / Deep Learning / Augmented Reality / Virtual Reality etc.)

11.Humanitarian, Public Policy and Legal Services

12.Communication

13.Education

14.Sustainable Development

15.Environment

16.Commerce, Medium and Small-Scale Industries

- Faculty Supervision:

Students are usually assigned an internal faculty guide/mentor who su- pervises their internship activities. This faculty member acts as a teacher, mentor, and critic, and ensures the internship aligns with academic goals. External Supervision: In many cases, an external expert from the host organization also guides the student.

- Documentation and Reporting:

1. Joining Report: To be submitted within a specified time frame (e.g., one week from joining).

2. Daily/Periodical Diary: Students are often required to maintain a daily or weekly record of their observations, work, and learning.

3. Internship Report: A comprehensive report detailing the work done, learning outcomes, and achievements during the internship. This report needs to be duly signed by the company official and faculty mentor.

4.Completion Certificate: Issued by the host organization upon successful completion

- Evaluation:

1.Evaluation is typically done by the institute, often within a short period after the internship ends.

2.It may involve presentations, viva-voce examinations, and assessment of the internship report and daily diary.

3.Performance-based feedback from the industry mentor is usually a key component

Savitribai Phule Pune University
Master of Engineering (2025 Course) – Electronics and Communication
(VLSI Design)

SEM-632-VLD - TECHNICAL SEMINAR II

Teaching Scheme	Credits	Examination Scheme
Practical: 06 Hours/Week	03	**Term Work** : 50 Marks **Practical** : 50 Marks

COURSE OBJECTIVE:

1. Deepen Technical Knowledge: To enable students to explore a specialized topic within Electronics and Communication Engineering beyond the regular curriculum, fostering in-depth understanding.
2. Develop Research Skills: To provide practical experience in identifying, acquiring, evaluating, and synthesizing information from various technical sources (research papers, standards, technical reports).
3. Enhance Communication Skills: To cultivate effective oral and visual presentation skills, enabling students to articulate complex technical concepts clearly and concisely to a knowledge- able audience.
4. Foster Critical Thinking: To encourage students to critically analyze existing research, identify challenges, propose solutions, and engage in constructive discussions.
5. Promote Independent Learning: To encourage self-directed learning and the ability to stay updated with emerging technologies and research trends.
6. Prepare for Thesis/Dissertation: To serve as a foundational step for the Master's thesis/dissertation, allowing students to explore potential research areas

COURSE OUTCOME:

On completion of the course, student will be able to:

1. **Formulate** the goals and objectives of scientific research.
2. Search, evaluate and **analyze** information about the achievements of science and technology in the target area and beyond.
3. **Interpret** data from different fields of science and technology.
4. **Build** the logic of reasoning and statements.
5. **Create**, design and edit text documents in accordance with the requirements of the organization or publisher

COURSE DESCRIPTION

The seminar aims to enhance students' research, presentation, and critical thinking skills, preparing them for advanced academic pursuits and professional careers

GUIDELINES

- **Responsibility of the students**

– The Seminar should be carried out individually by each student.

– A student should identify the area or topics in recent trends and developments in consul- tation with the guide

– A student should report to his/her respective guide regularly (at least once in a week) and report the progress of the seminar work.

– A student should follow the timelines and deadlines and inform the supervisor in case of any difficulty/delay.

– Students should maintain the record of all the meetings, remarks given by guide/reviewers and progress of the work in the project diary. The project diary must be presented during each review presentation to the reviewers.

– A student should conduct the research ethically, adhere to the academic integrity stan- dards, and cite sources whenever using any existing results

– A student should Incorporate constructive feedback to improve the quality and rigor of the research

– For final examination, students should complete the Seminar Report in all aspects including formatting and citation.

– Each student should prepare the report, get it approved by his/her guide and submit the duly signed copy within the deadline.

– A student should invest time and effort in preparing for seminar presentations and the oral defense of the seminar

- **Topic Selection**

– Relevance: Topics must be directly related to Computer Engineering, encompassing cur- rent research trends, emerging technologies, advanced concepts, or interdisciplinary applications.

– Scope: The topic should be sufficiently focused to allow for in-depth exploration within the seminar timeframe, yet broad enough to demonstrate a comprehensive understanding. Avoid overly narrow or excessively broad topics.

- Novelty (Desired): While not strictly a research paper, students are encouraged to explore topics that have recent advancements, open problems, or areas where their unique insights can be presented. Avoid merely summarizing introductory textbook material.

- Guide / Supervisor Approval: Each student must select a seminar topic in consultation with and obtain approval from an assigned faculty supervisor. The supervisor will guide the student in refining the topic and identifying relevant resources.

- Examples of Broad Areas: Artificial Intelligence/Machine Learning, Data Science & Big Data, Cybersecurity, Cloud Computing, Internet of Things (IoT), Computer Networks, Soft- ware Engineering, High-Performance Computing, Embedded Systems, Computer Vision, Natural Language Processing, Blockchain, Quantum Computing.

• **Seminar Structure and Deliverables** : The technical seminar typically involves the following stages and deliverables

- Topic Proposal (2-3 weeks after topic approval):
- A concise document (1-2 pages) outlining:
- Proposed Seminar Title
- Brief Description/Abstract of the Topic
- Motivation and Relevance to Computer Engineering
- Preliminary List of Key References (at least 5-7 reputable sources)
- Tentative Scope and Outline of the Presentation
- Submission: To the faculty supervisor for approval.
- Literature Review and Research (Ongoing): Sources: Students must primarily rely on peer-reviewed academic sources (IEEE Xplore, ACM Digital Library, SpringerLink, arXiv, Google Scholar), reputable conference proceedings, and established industry standards. Wikipedia and unverified blogs are generally not acceptable as primary sources.
- Critical Analysis: Beyond mere summarization, students are expected to critically

analyze the literature, identifying different approaches, their advantages/disadvantages, open issues, and potential future directions.

- Note-Taking & Organization: Maintain systematic notes and organize research material effectively.

- **Seminar Report/Paper (Due 2-3 weeks before presentation):**

- A written report (typically 15-25 pages, excluding references and appendices) detailing the seminar content.

- Format: Follow a professional academic paper format (e.g., IEEE transaction style).

- **Sections:**

- Abstract: A concise summary of the seminar topic and key findings.

- Introduction: Background, motivation, problem statement (if applicable), and outline of the report.

- Literature Review/Background: Detailed discussion of relevant concepts, theories, and existing work.

- Core Content: In-depth exploration of the chosen topic, presenting different methodologies, architectures, algorithms, or challenges as relevant.

- Analysis/Discussion: Critical evaluation of the presented material, comparing different approaches, discussing implications, and identifying gaps.

- Future Trends/Conclusion: Summarization of key takeaways, potential future directions, and concluding remarks.

- References: A comprehensive list of all cited sources, properly formatted

- Appendices (Optional): Supplementary material if necessary

- **Oral Presentation :**

- Duration: Typically, 25-30 minutes for presentation, followed by 10-15 minutes for Q&A. (Specific timings will be announced)

- Audience: Faculty members, peers, and potentially other interested individuals.

- Content: The presentation should effectively convey the key aspects of the

seminar topic. It should not simply be a reading of the report.

– Visual Aids: High-quality presentation slides (e.g., PowerPoint, Google Slides, LaTeX Beamer) are mandatory. Slides should be clear, concise, visually appealing, and support the oral de- livery. Avoid excessive text on slides.

– Delivery: Clear articulation, confident posture, good eye contact, and appropriate pace. Practice the presentation thoroughly.

– Q&A Session: Be prepared to answer questions from the audience on all aspects of the seminar topic. Demonstrate a strong understanding and ability to defend your perspectives.

- **Evaluation Criteria:** The technical seminar will be evaluated based on the following criteria:

– Topic Selection and Scope (10%): Relevance, timeliness, and appropriate depth of the chosen topic. Clarity and focus of the topic proposal.

– Literature Review and Research (25%): Breadth and depth of literature surveyed. Quality and credibility of sources used. Critical analysis and synthesis of information.

– Seminar Report/Paper (30%): Clarity, organization, and logical flow of content. Technical accuracy and depth of discussion. Adherence to academic writing standards (grammar, spelling, formatting, referencing). Originality in synthesis and critical insights. Absence of plagiarism.

– Oral Presentation (35%): Content: Clarity, completeness, and accuracy of the presented material. Organization: Logical flow, effective use of time. Visual Aids: Quality, clarity, and effectiveness of slides. Delivery: Confidence, clarity of speech, enthusiasm, engagement with the audience. Q&A: Ability to answer questions accurately, comprehensively, and confidently.

LEARNING RESOURCES:

Text Books:

1. "Engineering Communication" by Charles W. Knisely & Karin I. Knisely
2. "Technical Communication: Principles and Practice" by Meenakshi Raman & Sangeeta Sharma

3. "The Craft of Scientific Presentations" by Michael Alley

NPTEL/SWAYAM/MOOC:

1. https://nptel.ac.in/courses/109/106/109106180/
2. https://www.udemy.com/course/technical-writing/
3. https://www.edx.org/course/writing-in-the-sciences

Savitribai Phule Pune University
Master of Engineering (2025 Course) – Electronics and Communication
(VLSI Design)

SEM-632-VLD - TECHNICAL SEMINAR II

Teaching Scheme	Credits	Examination Scheme
Practical: 18 Hours/Week	09	**Term Work :** 25 Marks **Oral/ Presentation :** 25 Marks

COURSE OBJECTIVE:

1. Demonstrate an ability to plan a research project, such as is required in a research proposal prior to the launch of their work
2. Demonstrate an ability to comply with ethical, safety, and documentation processes appropriate to their project
3. Demonstrate expert knowledge in the subject of their research project, such as through an integrated literature survey
4. Demonstrate expert knowledge in the research methods appropriate to generating reliable data for their research questions
5. Demonstrate the ability to manage projects and to make constructive use of expertise associated with their project, while working as an independent learner
6. Demonstrate an ability to relate their original data to existing literature, or to create an novel synthesis of existing materials
7. Demonstrate an ability to assemble their findings into a substantial piece of writing that presents a clear thesis and a cohesive, evidence-based argument
8. Demonstrate an ability to balance description, analysis, and synthesis within their project report
9. Demonstrate an ability to reflect on the strengths and weaknesses of their research and method- ology, with constructive advice on how they might improve their efforts in future work

COURSE OUTCOME:

On completion of the course, student will be able to:

1. Demonstrate how to search the existing literature to gather information about a specific problem or domain.
2. Identify the state-of-the-art technologies and research in the chosen domain, and high-light open problems that are relevant to societal or industrial needs.

3. Evaluate various solution techniques to determine the most feasible solution within given constraints for the chosen dissertation problem.
4. Apply software engineering principles related to requirements gathering and design to produce relevant documentation.
5. Write a dissertation report that details the research problem, objectives, literature review, and solution architecture

COURSE DESCRIPTION

The master's degree culminates in a research project of the student's own design. This research project is documented by a final research report or dissertation. The student's work is guided by an academic supervisor. Students are expected to choose real-world contemporary problem and apply the engineering principles learned, to solve the problem through building prototypes or simulations or writing codes or establishing processes/synthesis/correlations etc. Students are expected to construct a research project that includes original research, deliberate and well considered methodological choices, and shows relevance to significant conversations within the discipline. The dissertation should represent the very best research and analysis a student can produce.

GUIDELINES

General Guidelines:

(a) The dissertation is a year-long project, conducted and evaluated in two phases. It can be carried out either in-house or within an industry as assigned by the department. The project topic and internal advisor (a faculty member from the department) are determined at the beginning of Phase I.

(b) Student is expected to complete the following activities in Phase-I:

i. Literature survey

ii. Problem Definition

iii. Motivation for study and Objectives

iv. Preliminary design / feasibility / modular approaches

v. Design of the research project

Phase 1: Informal conversations

Students are strongly encouraged to discuss possible research project ideas with the internal guide, fellow students, and other research professionals. All research projects begin with

open-ended conversations and scoping exercises. These should be non-committal.

Phase 2: Identify topic

The first formal step in the module involves identifying a preliminary project title and writing an abstract of no more than 200 words. This requires submitting a completed registration form. Writing an abstract for a research proposal or for completed research work is an important transferable skill. Students who do not submit a completed registration form will be assigned a project. The project title is understood to be provisional. Supervisors will be assigned to students after the project title/ abstract forms have been submitted. Supervision: A supervisor is required. The main responsibilities of the supervisor are to assist the student with project management and to advise the student on criteria for assessment. You can expect your supervisor to read and comment on a full draft of your research proposal and of your project. It is a good idea to discuss a time line for your project with your supervisor, and to establish a definite timetable.

Some key points in our advice to students on compliance:

1. Allow at least two weeks between submitting an ethics application and the date of your first data collection
2. The supervisor must approve (and sign!) your ethics application before you submit it at departmental level
3. After your protocols have been approved, append a copy of your ethical approval certificate to the dissertation and project proposal.

Phase 3: Project proposal

The proposal should reflect a student's best effort. At the same time, we recognize research often raises new questions. Some redefinitions of topics and titles is common later in the research process. Students should keep their supervisors up to date on these developments, and they can expect a reasonable amount of adaptation.

Phase 4: Term-1 Research

Students are expected to commit substantial time during the term to their research project. Supervisions The principal form of academic input for the research project normally comes through discussions with the designated supervisor. The majority of these meetings should be face-to-face, either in person or via video- or audio-conferencing technology.

Students are expected to respect these periods of absence and plan their needs accordingly. One distinction is crucial:

(1) When staff are on leave, they are off work (i.e., not expected to maintain contact with their supervisees or to undertake their duties); however,

(2) When staff are working remotely, they are at work (i.e., expected to maintain contact and to be available for normal duties).

A student's supervisor is not the only person who may advise on projects and writing. Others include peers and subject experts

Phase 5: Submit project report

The project report with the specific due date must be submitted to Department

Additional Information

- **Research notebook:** Students are strongly advised to maintain a research notebook, either digital or paper, and to keep this up to date. A research notebook can prove useful should examiners query research methods, research integrity, or research process.
- **Preventing data loss:** Protect yourself against loss of research material and writing by maintaining a system for secure, redundant, up-to-date back-up of research material and writing. Loss cannot be accepted as a reason for failing to meet a deadline. A copy of written notebooks can be stored by supervisors for the duration of the project. Loss of project materials through accidents and theft have occurred in the past; these have had devastating effects on the unprepared. All students are warned to create redundancies to protect their project from similar calamities.
- **Extensions:** This is a long-term research project, and time management is a learning objective. Short-term extensions normally are not considered. Applications for extension must be made through the processes described in the STS Student Handbook. Personal Tutors are the first point of contact on extension requests.
- **Word counts:** Words counted towards the total word count include the main body of the report and supporting footnotes or endnotes. The word count does not include: bibliography, front matter (title page, keywords, abstract, table of contents, acknowledgments), appendix material, supplemental data packages, table and figure legends, or documentation of ethics protocols or approvals. Otherwise, University standard policy on word counts will apply.
- **Re-using coursework from other modules:** Text and ideas in the research proposal may reappear in the dissertation if significantly developed or further elaborated; however, Universities policy on self-plagiarism prevents the same work receiving credit twice. This means rote duplication is not allowed.
- **Citation format:** The style must be clear, explicit, and meaningful. In every instance, it must

allow an examiner to locate efficiently and specifically material referred to. As a recommendation, students should use a style frequently used in the literature relevant to their research project. Most journals have style guides in their notes to contributors. Students should dis- cuss options with their supervisors, and they should keep in mind that efficient citation is one element in the criteria for assessment.

Savitribai Phule Pune University, Pune

Maharashtra, India

ME (2025 Course) – Electronics & Communication (VLSI Design)

Semester IV

Savitribai Phule Pune University
Master of Engineering (2025 Course) – Electronics and Communication
(VLSI Design)

SEM-671-VLD - TECHNICAL SEMINAR III

Teaching Scheme	Credits	Examination Scheme
Practical: 08 Hours/Week	03	**Term Work** : 50 Marks **Oral/ Presentation**: 50 Marks

COURSE OBJECTIVE:

1. Deepen Technical Knowledge: To enable students to explore a specialized topic within Electronics and Communication Engineering beyond the regular curriculum, fostering in-depth understanding.
2. Develop Research Skills: To provide practical experience in identifying, acquiring, evaluating, and synthesizing information from various technical sources (research papers, standards, technical reports).
3. Enhance Communication Skills: To cultivate effective oral and visual presentation skills, enabling students to articulate complex technical concepts clearly and concisely to a knowledge- able audience.
4. Foster Critical Thinking: To encourage students to critically analyze existing research, identify challenges, propose solutions, and engage in constructive discussions.
5. Promote Independent Learning: To encourage self-directed learning and the ability to stay updated with emerging technologies and research trends.
6. Prepare for Thesis/Dissertation: To serve as a foundational step for the Master's thesis/dissertation, allowing students to explore potential research areas

COURSE OUTCOME:

On completion of the course, student will be able to:

1. **Formulate** the goals and objectives of scientific research.
2. Search, evaluate and **analyze** information about the achievements of science and technology in the target area and beyond.
3. **Interpret** data from different fields of science and technology.
4. **Build** the logic of reasoning and statements.
5. **Create**, design and edit text documents in accordance with the requirements of the organization or publisher

COURSE DESCRIPTION

The seminar aims to enhance students' research, presentation, and critical thinking skills, preparing them for advanced academic pursuits and professional careers

GUIDELINES

- **Responsibility of the students**

– The Seminar should be carried out individually by each student.

– A student should identify the area or topics in recent trends and developments in consultation with the guide

– A student should report to his/her respective guide regularly (at least once in a week) and report the progress of the seminar work.

– A student should follow the timelines and deadlines and inform the supervisor in case of any difficulty/delay.

– Students should maintain the record of all the meetings, remarks given by guide/reviewers and progress of the work in the project diary. The project diary must be presented during each review presentation to the reviewers.

– A student should conduct the research ethically, adhere to the academic integrity standards, and cite sources whenever using any existing results

– A student should Incorporate constructive feedback to improve the quality and rigor of the research

– For final examination, students should complete the Seminar Report in all aspects including formatting and citation.

– Each student should prepare the report, get it approved by his/her guide and submit the duly signed copy within the deadline.

– A student should invest time and effort in preparing for seminar presentations and the oral defense of the seminar

- **Topic Selection**

– Relevance: Topics must be directly related to Computer Engineering, encompassing cur- rent research trends, emerging technologies, advanced concepts, or interdisciplinary applications.

– Scope: The topic should be sufficiently focused to allow for in-depth exploration within the seminar timeframe, yet broad enough to demonstrate a comprehensive understanding. Avoid overly narrow or excessively broad topics.

– Novelty (Desired): While not strictly a research paper, students are encouraged to explore topics that have recent advancements, open problems, or areas where their unique insights can be presented. Avoid merely summarizing introductory textbook material.

– Guide / Supervisor Approval: Each student must select a seminar topic in consultation with and obtain approval from an assigned faculty supervisor. The supervisor will guide the student in refining the topic and identifying relevant resources.

– Examples of Broad Areas: Artificial Intelligence/Machine Learning, Data Science & Big Data, Cybersecurity, Cloud Computing, Internet of Things (IoT), Computer Networks, Soft- ware Engineering, High-Performance Computing, Embedded Systems, Computer Vision, Natural Language Processing, Blockchain, Quantum Computing.

• **Seminar Structure and Deliverables** : The technical seminar typically involves the following stages and deliverables

– Topic Proposal (2-3 weeks after topic approval):

– A concise document (1-2 pages) outlining:

– Proposed Seminar Title

– Brief Description/Abstract of the Topic

– Motivation and Relevance to Computer Engineering

– Preliminary List of Key References (at least 5-7 reputable sources)

– Tentative Scope and Outline of the Presentation

– Submission: To the faculty supervisor for approval.

– Literature Review and Research (Ongoing): Sources: Students must primarily rely on peer-reviewed academic sources (IEEE Xplore, ACM Digital Library, SpringerLink, arXiv, Google Scholar), reputable conference proceedings, and established industry standards. Wikipedia and unverified blogs are generally not acceptable as primary sources.

– Critical Analysis: Beyond mere summarization, students are expected to critically analyze the literature, identifying different approaches, their advantages/disadvantages, open issues, and potential future directions.

– Note-Taking & Organization: Maintain systematic notes and organize research

material effectively.

- **Seminar Report/Paper (Due 2-3 weeks before presentation):**

– A written report (typically 15-25 pages, excluding references and appendices) detailing the seminar content.

– Format: Follow a professional academic paper format (e.g., IEEE transaction style).

- **Sections:**

– Abstract: A concise summary of the seminar topic and key findings.

– Introduction: Background, motivation, problem statement (if applicable), and outline of the report.

– Literature Review/Background: Detailed discussion of relevant concepts, theories, and existing work.

– Core Content: In-depth exploration of the chosen topic, presenting different methodologies, architectures, algorithms, or challenges as relevant.

– Analysis/Discussion: Critical evaluation of the presented material, comparing different approaches, discussing implications, and identifying gaps.

– Future Trends/Conclusion: Summarization of key takeaways, potential future directions, and concluding remarks.

– References: A comprehensive list of all cited sources, properly formatted

– Appendices (Optional): Supplementary material if necessary

- **Oral Presentation :**

– Duration: Typically, 25-30 minutes for presentation, followed by 10-15 minutes for Q&A. (Specific timings will be announced)

– Audience: Faculty members, peers, and potentially other interested individuals.

– Content: The presentation should effectively convey the key aspects of the seminar topic.It should not simply be a reading of the report.

– Visual Aids: High-quality presentation slides (e.g., PowerPoint, Google Slides, LaTeX Beamer) are mandatory. Slides should be clear, concise, visually appealing, and support the oral de- livery. Avoid excessive text on slides.

- Delivery: Clear articulation, confident posture, good eye contact, and appropriate pace.Practice the presentation thoroughly.

- Q&A Session: Be prepared to answer questions from the audience on all aspects of the seminar topic. Demonstrate a strong understanding and ability to defend your perspectives.

- **Evaluation Criteria:** The technical seminar will be evaluated based on the following criteria:

- Topic Selection and Scope (10%): Relevance, timeliness, and appropriate depth of the chosen topic. Clarity and focus of the topic proposal.

- Literature Review and Research (25%): Breadth and depth of literature surveyed. Quality and credibility of sources used. Critical analysis and synthesis of information.

- Seminar Report/Paper (30%): Clarity, organization, and logical flow of content. Technical accuracy and depth of discussion. Adherence to academic writing standards (grammar, spelling, formatting, referencing). Originality in synthesis and critical insights. Absence of plagiarism.

- Oral Presentation (35%): Content: Clarity, completeness, and accuracy of the presented material. Organization: Logical flow, effective use of time. Visual Aids: Quality, clarity, and effectiveness of slides. Delivery: Confidence, clarity of speech, enthusiasm, engagement with the audience. Q&A: Ability to answer questions accurately, comprehensively, and confidently.

LEARNING RESOURCES:

Text Books:

1. "Engineering Communication" by Charles W. Knisely & Karin I. Knisely
2. "Technical Communication: Principles and Practice" by Meenakshi Raman & Sangeeta Sharma
3. "The Craft of Scientific Presentations" by Michael Alley

NPTEL/SWAYAM/MOOC:

1. https://nptel.ac.in/courses/109/106/109106180/
2. https://www.udemy.com/course/technical-writing/

3. https://www.edx.org/course/writing-in-the-sciences

Savitribai Phule Pune University
Master of Engineering (2025 Course) – Electronics and Communication
(VLSI Design)

RP-681-VLD- RESEARCH PROJECT STAGE - II

Teaching Scheme	Credits	Examination Scheme
Practical: 36 Hours/Week	09	**Term Work :** 150 Marks **Oral/ Presentation : 50** Marks

COURSE OBJECTIVE:

1. **Demonstrate** an ability to plan a research project, such as is required in a research proposal prior to the launch of their work
2. **Ability** to manage projects and to make constructive use of expertise associated with their project, while working as an independent learner
3. **Ability** to relate their original data to existing literature, or to create an novel synthesis of existing materials
4. **Identify** and **formulate** a problem of research interest in the chosen area of computing.

COURSE OUTCOME:

On completion of the course, student will be able to:

1. **Undertake** independent research that makes an original contribution to knowledge, or produces a novel synthesis of existing materials relevant to significant conversations in the discipline
2. **Plan** their project in advance, using a proposal to describe their undertaking, describe how it will be managed, and reflect upon its value
3. **Relate** their original research to existing literature on the subject and relate their work to general themes in their relevant scholarly literature
4. **Assemble** their rationale, methods, findings, and analysis into a substantial piece of writing that presents a clear thesis and a cohesive evidence-based argument or analysis
5. **Reflect** on the strengths and weaknesses of their research and methodology, understanding how they might improve their efforts in future work

COURSE DESCRIPTION

The master's degree culminates in a research project of the student's own design. This project is documented by a final research report or dissertation. The student's work is

guided by an supervisor or guide. Students are expected to construct a research project that includes original research, deliberate and well considered methodological choices, and shows relevance to significant conversations within the discipline. The dissertation should represent the very best research and analysis a student can produce. Study of relevant supplementary literature, mastering useful programming languages and tools for the problem, are also expected at this stage of the project.

GUIDELINES

General Guidelines

- The student shall consolidate and complete the remaining part of the research work started in Semester III. This will consist of Selection of Technology, Installations, implementations, testing, Results, measuring performance, discussions using data tables per parameter considered for the improvement with existing/known algorithms/systems, comparative analysis, validation of results and conclusions.
- The student shall prepare the duly certified final report of dissertation in standard format for satisfactory completion of the work by the concerned guide and head of the Department/Institute.
- The students are expected to validate their study undertaken by publishing it at standard platforms.
- The investigations and findings need to be validated appropriately at standard platforms like conference and/or peer reviewed journal.
- The student has to exhibit continuous progress through regular reporting and presentations and proper documentation of the frequency of the activities in the sole discretion of the PG coordination/Head of the department. The continuous assessment of the progress needs to be documented unambiguously.
- Supervisor Interaction: Minimum one meeting per week.
- Logbook: Maintain a record of work progress and supervisor comments.
- Ethics: No plagiarism, false results, or unethical practices allowed.
- Backup: Keep source code, datasets, and reports backed up securely.
- Submission Format: Soft copy (PDF) + Hard copy as per institute norms.

KEY COMPONENTS:

Implementation

∗ Complete development/simulation/testing of the system or model.

* Ensure correctness, efficiency, and validation of results.

Results & Analysis

* Include experimental setup, datasets used, and performance metrics.
* Graphs, tables, and comparison with existing techniques.
* Highlight key findings and their significance.

Conclusion and Future Work

* Summarize outcomes, contributions, and applications.
* Suggest extensions or improvements for future research.

Paper Publication

* At least one paper (optional/encouraged) in peer-reviewed conference/journal.
* Attach publication/proof as appendix (if available).

Final Report Format

* Revised version of Stage 1 report with added implementation, results, and conclusion chapters.
* Maintain academic writing standards and include all necessary references.

Plagiarism Report

* Final version must again be checked and should not exceed 15% similarity.

Evaluation Parameters

* Completeness and quality of implementation
* Analysis and originality of results
* Quality of documentation and adherence to format
* Viv-voce performance and clarity of understanding
* Contribution to knowledge or innovation

Task Force for Curriculum Design and Development

Programme Coordinator

Dr. M. B. Mali - Member, Board of Studies – E&TC Engineering

Team Members for Course Design

Dr. Swati Gandhi, Anatrao Pawar College of Engineering and Resaerch, Pune
Dr. Neha Shahare, KJ College of Engineering & Management Research, Pune
Prof. Snehal Veer, Anatrao Pawar College of Engineering and Resaerch, Pune
Prof. Sharad Jagtap, Anatrao Pawar College of Engineering and Resaerch, Pune
Dr.Amar Deshmukh, Anatrao Pawar College of Engineering and Resaerch, Pune
Dr. Sunita S. Lokhande, Sinhgad College of Engineering, Pune

Chairman

Dr. Suresh Shirbahadurkar - Board of Studies - Electronics & Telecommunication Engineering
Savitribai Phule Pune University, Pune

Dean

Dr. Pramod Patil - Dean – Science and Technology
Savitribai Phule Pune University, Pune