

SAVITRIBAI PHULE PUNE UNIVERSITY

(Formerly University of Pune)



EXAMINATION CIRCULAR NO.437 OF. 2023

**SECOND YEAR M.E. ELECTRONICS & TELECOMMUNICATION (VLSI & EMBEDDED
SYSTEMS) (2013 PAT.)**

Examination of Oct/Nov/Dec-2023 (No Equivalence)

(Under Faculty of SCIENCE AND TECHNOLOGY : B)ENGINEERING)

INSTRUCTIONS FOR CANDIDATES

- Candidates are required to be present at the examination centre, THIRTY MINUTES before the time fixed for paper.
- Candidates are forbidden from taking any material into the examination hall, that can be used for malpractice at the time of examination.
- Candidates are requested to see the Notice Board at their place of examination regularly for changes if any, that may be notified later in the program.
- No request for any special concession such as a change in time or any day fixed for the University Examination on any ground shall be granted.
- Candidates are requested to note the Day, Date and Time of every Paper on every day.
Candidates are permitted to use stencils at the time of examination.
- Candidates appearing for the examinations are expected to provide themselves with Side- rules.
- The exchange or loan of side-rules, drawing instruments of other materials used in the examination hall is Not Permitted while the examinations are in process.
- Candidates must bring their own instruments and will not be allowed to borrow from each other under any circumstances.
- Use of non-programmable battery operated electronic Calculator of Pocket-size is allowed. The exchange of Calculators is not allowed.
- The written examination will be conducted in the following order.

**SECOND YEAR M.E. ELECTRONICS &
TELECOMMUNICATION (VLSI & EMBEDDED
SYSTEMS) (2013 PAT.)/437/S-2023**

SEMESTER - III

Time:-10.00 AM To 01.00 PM

Day & Date	Paper Code	Subject
Monday 01-01-2024	604201	FAULT TOLERANT SYSTEMS

Ganeshkhind, Pune - 411 007

Ref.No/XCT:1410

Date:18/12/2023

Director,

Board of Examinations and Evaluation